COMMUNICATION SCHEDULE OPTIMIZATION OF CASCADE CONTROL USING FOUNDATION FIELDBUS

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Abstract. *This paper presents a technique to optimize the communication schedules generated for synchronization of Foundation Fieldbus H1 devices in cascade control loop. A level-to-flow cascade control operated by the Harmonas-DEO host system is examined as an illustrative case study. Major objectives of the optimization are not only to minimize the latency of the control loop but also to maximize the availability of the network bandwidth. The proposed technique can be applied for H1 segment macrocycle schedules performing the control functions in both of the host controller and the field devices. Three examples for optimizing communication schedules generated from different control block assignments are described. The validation of the optimization methods can be determined by using two metrics: control loop latency improvement and publication gap availability improvement. Experimental results confirm that the proposed technique works effectively to operate the studied H1 segment for cascade control without any problems.*
Keywords: Foundation Fieldbus, Cascade control, Communication schedule, Macrocycle, Control latency, Optimization

1. **Introduction.** A fieldbus is a method for digital communication in the shop floor or process plant in which there is distributed and programmable intelligence at each network node. Since the advent of digital communication technology, several fieldbuses have been developed to serve particular sectors of the automation industry. Fieldbuses for hydrocarbon processing plants dominated in continuous regulatory control were designed to connect smart field instruments to each other and to higher level control networks. A process control based upon constant sampling intervals does demand tight time synchronization between devices forming control loop. Time synchronization cannot be obtained without a synchronous network. Foundation Fieldbus (FF) is uniquely different from other fieldbuses available for use in process industry in that its standard includes the definition of software function blocks for making it possible to distribute control strategies into smart field instruments [1]. Scheduling of function block execution and communication is an effective method to coordinate the control strategies distributed in different devices connected on the network. There is one schedule, frequently called segment macrocycle, for each FF H1 network in the system. The schedule is automatically generated by a configuration tool and downloaded to the host and the devices as part of the control strategy. Nevertheless, the schedule optimization is still required for improving system performance [2]. In addition, scheduling of the segment macrocycle depends on several factors such

as number and type of field devices, scheme of control loops, and allocation of control function blocks. Among previously reported methods to achieve optimal communication schedules on FF H1 networks [3-5], none of them concentrates on practical technique for optimizing segment macrocycle for cascade control loop in which primary and secondary control function blocks can be assigned in either the host controller or field devices.

This paper aims to propose a technique to practically optimize the communication schedules during system engineering phase for cascade control strategy using FF technology. Optimization methods for three different cases of control block assignment by using the Harmonas-DEO as the configuration tool are described. The first studied case is the optimization of the schedule generated for running the control function blocks in the host controller, while the other two cases are the optimizations of the schedules generated for running the control function blocks in the field instruments. In order to evaluate the schedule improvements numerically, two metrics named control loop latency improvement and publication gap availability improvement are employed. Experimental results from the real H1 segment operation by using non-optimized schedule and optimized schedule in the case of assigning control function blocks with two external links are also included and compared.

The remainder of the paper is organized as follows. In Section 2, a brief description of cascade control using FF technology and communications on H1 network is given. A case study of level-to-flow cascade control is described in Section 3. The proposed technique is presented in Section 4. Some experimental results are given and discussed in Section 5, and then the conclusions are made in Section 6.

2. **FF-Based Cascade Control Loop and Communications on H1 Network.**

2.1. **Cascade control using FF.** The cascade control loop can be established by configuring a series of software function blocks as shown in Figure 1 [2]. This control scheme has two input class blocks (AI1 and AI2), two control class blocks (PID1 and PID2), and one output class block (AO1). Input class blocks and output class blocks are connected to sensor hardware and to actuator hardware, respectively, via transducer blocks over a channel specified by channel parameter. Control class blocks are used to perform closed-loop control, and they have back-calculation functionality to provide bumpless mode transfers and reset windup protection. A list of the blocks used with their function in normal operating mode and execution order is summarized in Table 1. The blocks are linked to each other from output parameters to input parameters and executed sequentially. Links between function blocks in different devices, referred to as 'external links', are communicated over the H1 network, whereas links between function blocks within the same device, referred to as 'internal links', do not have to be communicated on the network. Figure 2 shows three different cases of assigned control locations for function blocks for cascade control loop, where dashed line rectangles indicate function blocks within a single device. From
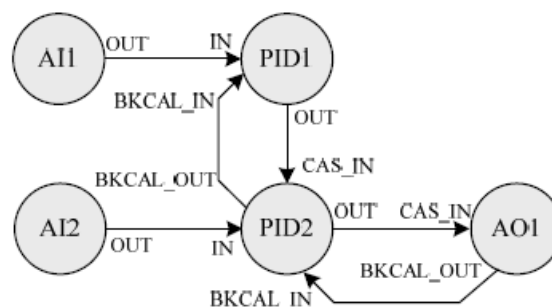

FIGURE 1. Cascade control strategy using FF function blocks

TABLE 1. FF function blocks used for building cascade control strategy

| Block	Normal mode	Function required in process control
Primary analog input block (AI1)	Automatic	Converting the primary measuring signal into a numerical value
Secondary analog input block (AI2)	Automatic	Converting the secondary measuring signal into a numerical value
Primary PID control block (PID1)	Automatic	Receiving the operator-entered setpoint as well as the measurement value from the primary AI1 output, and calculating the block output
Secondary PID control block (PID2)	Cascade	Receiving its cascade setpoint from the primary PID1 output as well as the measurement value from the secondary AI2 output, and calculating the block output
Analog output block (AO1)	Cascade	Fetching and scaling the secondary PID2 output, and passing to the transducer block for valve actuation

(a) Case 1

(b) Case 2

(c) Case 3
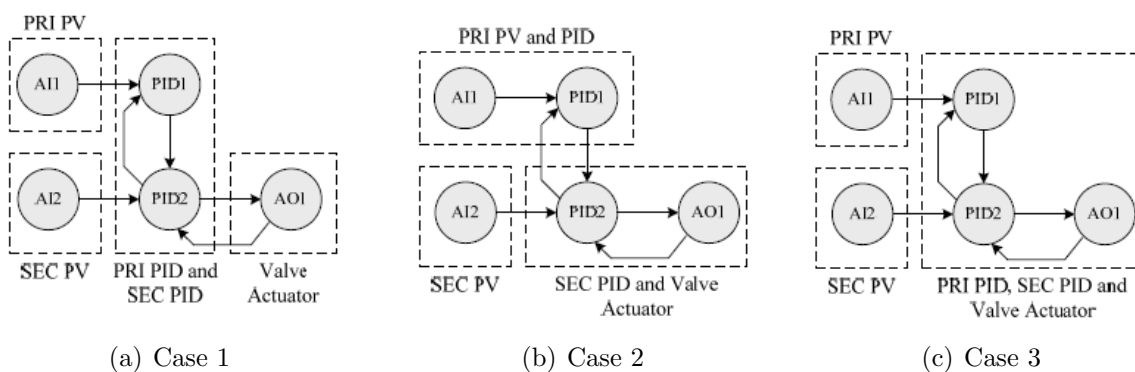
FIGURE 2. Alternative locations for control block assignment for cascade control loop

Figure 2(a), both of the PID1 and PID2 blocks are assigned in the host controller with the traditional distributed control system (DCS) approach. This configuration requires four external links, if the block output is to be transmitted on the H1 network. An alternative with three external links is for the PID1 block to be in its analog input transmitter and the PID2 and AO blocks to be in the valve positioner as shown in Figure 2(b). However, if the valve positioner supports two PID function blocks, a configuration with two external links is that both the PID1 and PID2 blocks are located in the valve positioner as shown in Figure 2(c).

2.2. **Communications on FF H1 network [1,2].** There are three types of data transmission occurred on H1 network: hard periodical communication, soft periodical communication, and aperiodic communication [6]. The hard periodical communication is provided for scheduled process data transmission shown in Figure 2 on the network by using publisher-subscriber model. Based on client-server model or report distribution model, the soft periodical communication is used for unscheduled data transmission on a cyclic basis, whereas the aperiodic communication is offered for infrequent data transmission of unscheduled events. When building control loop strategy, the schedule or segment macrocycle for function block executions and external link communications is produced by the configuration tool. The data transmission on H1 network is controlled by the link active scheduler (LAS). The LAS maintains the communications based on the segment macrocycle and token-passing mechanism to ensure that only one device at a time is granted permission to access the network. When the block output is scheduled for transmission, the LAS issues a compel data (CD) message to the device. When receiving such message,

the device publishes the specified process data to all devices on the segment configured to receive the data. When the LAS detects a communication gap large enough to transfer unscheduled data, it sends the pass token (PT) message to the devices sequencially. Once the device receives the PT command, it can send the data until it is finished or until the maximum token hold time is expired, whichever is shorter. If the LAS determines that the time remaining between the return of the token and the next CD command is too short to allow for unscheduled transmission or link maintenance messages, the LAS holds the token and may issue idle messages if required to prevent too long silent time, and then sends the CD command.

3. **Case Study with Level-to-Flow Cascade Control.** Figure 3 shows the system architecture of the case study with level-to-flow cascade control using FF system. Three H1 field devices used in control loop are level transmitter modeled EJX110A from Yokogawa (LIT_101), flow transmitter modeled 8732E from EPM (FIT_101), and valve positioner modeled AVP303 from Azbil (FCV_101). The Harmonas-DEO system distributed by Azbil is the integrated host with capabilities to configure and operate the FF segments.

Table 2 gives major function block details, number of block, and block execution time of the field devices used for building cascade control loop by using the Harmonas-DEO system. The function block allocation in the H1 field instruments used for configuring the control loops of Figure 2 is summarized in Table 3.
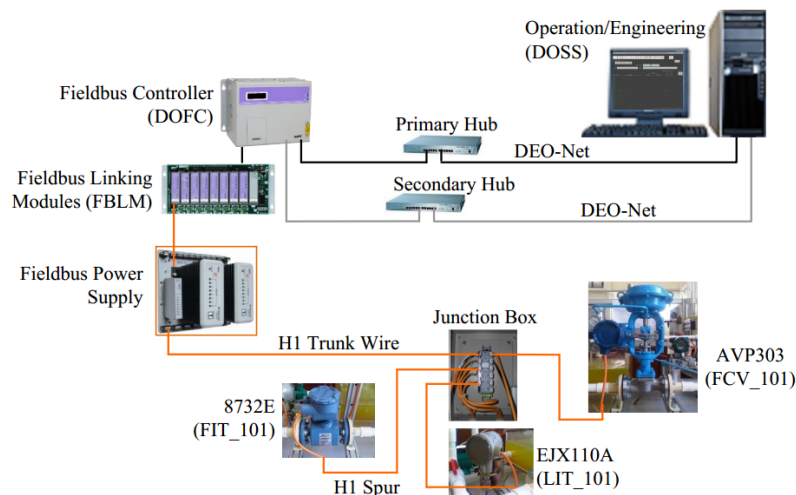

FIGURE 3. Case study with level-to-flow cascade control using FF system

TABLE 2. Function block details for building control loop by using the Harmonas-DEO

PD-Tag	AI Count	AI Time	PID Count	PID Time*	AO Count	AO Time*
LIT_101	3	30 ms	1	50 ms	N/A	N/A
FIT_101	1	10 ms	1	15 ms	N/A	N/A
FCV_101	N/A	N/A	2	130 ms	1	80 ms

*The block execution time includes extra time required by the host used of 5 ms.

TABLE 3. Function block allocation for configuring control loops of Figure 2

Case	AI1	AI2	PID1	PID2	AO1
1	LIT_101	FIT_101	Host Controller	Host Controller	FCV_101
2	LIT_101	FIT_101	LIT_101	FCV_101	FCV_101
3	LIT_101	FIT_101	FCV_101	FCV_101	FCV_101

4. **Proposed Technique.** Generally, the natural or non-optimized schedule is generated by specifying function blocks to be executed in order of input class block, control class block, and output class block as well as by positioning data transfers for external function block links to occur instantly after the upstream blocks completed their execution.

4.1. **Optimizing communication schedules from the case study.** In order to optimize the segment macrocycle, which is a significant component in control loop dynamics, for better performance of cascade control, there are two opportunities as follows.

- Minimizing control loop latency by scheduling the primary AI1 and secondary AI2 blocks to be executed in parallel. The AI1 and AI2 blocks are distributed into separated devices, LIT_101 and FIT_101, respectively, so these blocks are independent functions.

- Maximizing the availability of the segment macrocycle for unscheduled communication by grouping the data transfers for external function block links successively, whenever possible.

To minimize control loop latency, the natural schedule with 4 external links of Case 1 is optimized by assigning the AI1 and AI2 blocks to be executed in parallel as shown in Figure 4. It should be noted that these schedules exclude the execution times of the PID blocks located in the host controller. In addition, the execution of the host PID algorithm is not commonly synchronized with the execution of the segment macrocycle.

Similarly, the natural schedule with 3 external links of Case 2 is improved for latency reduction by scheduling the AI1 and AI2 blocks to be executed concurrently as illustrated in Figure 5.

The natural schedule with 2 external links of Case 3 is optimized by scheduling the AI1 and AI2 blocks to be executed simultaneously as well as by grouping two scheduled communications consecutively to publish the outputs of the AI1 and AI2 blocks as displayed in Figure 6.
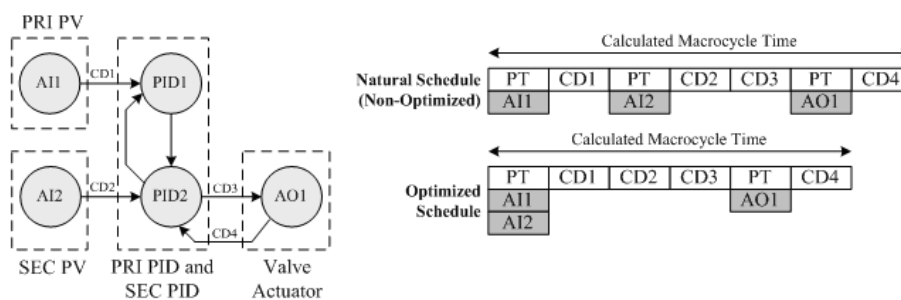

FIGURE 4. Optimizing the schedule for running the configured control loop of Case 1
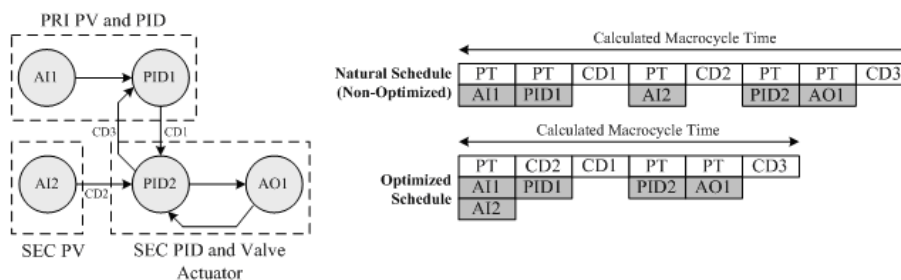

FIGURE 5. Optimizing the schedule for running the configured control loop of Case 2
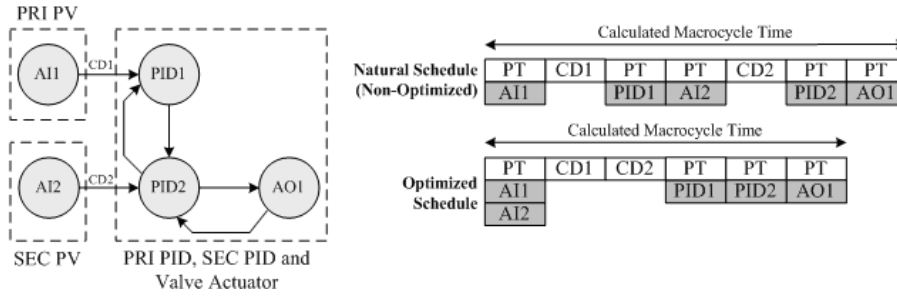
FIGURE 6. Optimizing the schedule for running the configured control loop of Case 3

4.2. Evaluation of the validation of the proposed technique.

In order to evaluate the validation of the proposed technique for optimizing the communication schedules, two following metrics are applied [4].

Control Loop Latency Improvement (CLLI) – Control loop latency is a period of time between the input processing and the output processing of the control sequence. The control sequence duration can be determined by the time interval that the AI1 block is initiated to execute until the AO1 block completes its execution or the end of CD after the AO1 (if needed). This metric can be expressed as:

$$CLLI = \left(1 - \left(\frac{optimized\_control\_sequence\_duration}{natural\_control\_sequence\_duration} \right) \right) \times 100\% \qquad (1)$$

Publication Gap Availability Improvement (PGAI) – Publication gap is the time between the end of scheduled publication to the start of the next publication. The usable publication gap means the gap between scheduled data publications that is greater than the minimum time needed for any other communications. If the minimum time needed for any communications is 30 ms, then the publication gap will be available when it is greater than 30 ms. This metric can be stated as:

$$PGAI = \left(1 - \left(\frac{\sum (length\_natural\_usable\_gap)}{\sum (length\_optimized\_usable\_gap)} \right) \right) \times 100\% \qquad (2)$$

5. Results and Discussion.

The Harmonas-DEO host system was utilized to configure the field devices and control loops as well as to operate the studied H1 segment. Experimental results from building the cascade control loops using the proposed technique to optimize the communication schedules are summarized in Table 4, where the default value for each scheduled data transmission used by the scheduling function in the host is 30 ms, and the requested macrocycle for operating the studied H1 segment is 1,000 ms. Figure 7 shows the macrocycles produced by the Harmonas-DEO for the control loop with the assignment of PID blocks of Case 3.

TABLE 4. Experimental results from optimizing the schedules of three different cases

| Item	Case 1	Case 2	Case 3
Calculated Macrocycle of Non-optimized Schedule	240 ms	390 ms	440 ms
Calculated Macrocycle of Optimized Schedule	230 ms	350 ms	400 ms
Scheduled Communication Load during Calculated Macrocycle of Optimized Schedule	52.174%	25.714%	15.000%
Control Loop Latency Improvement	4.167%	10.256%	9.091%
Publication Gap Availability Improvement	1.220%	1.176%	3.297%
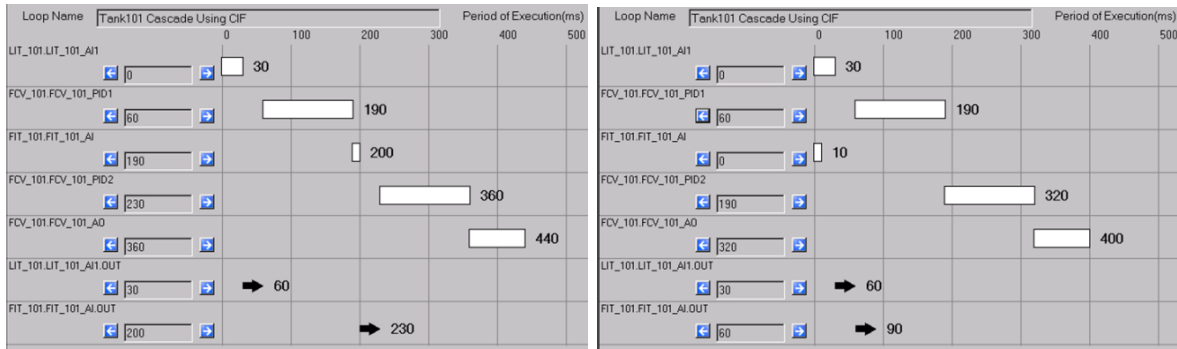
(a) Non-optimized macrocycle

(b) Optimized macrocycle

FIGURE 7. Macrocycles produced by the Harmonas-DEO for the control loop of Case 3
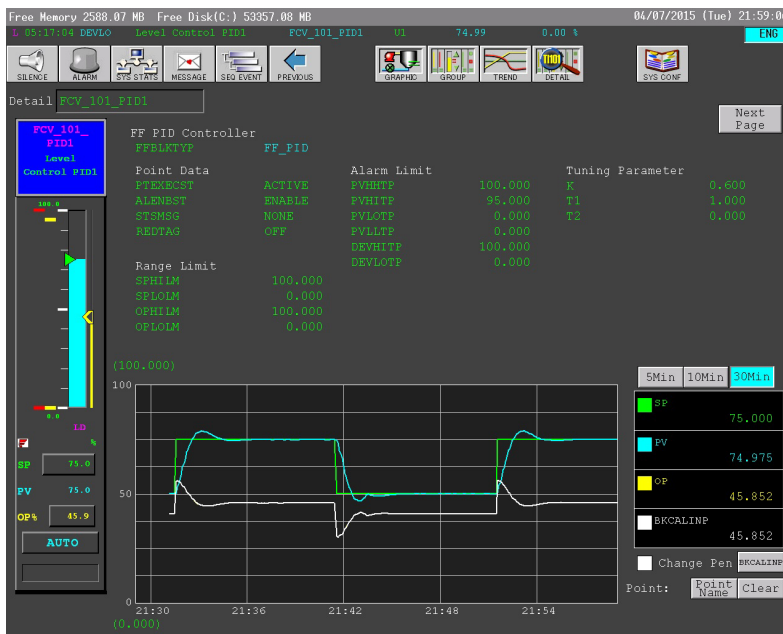
(a) Case of Figure 7(b)
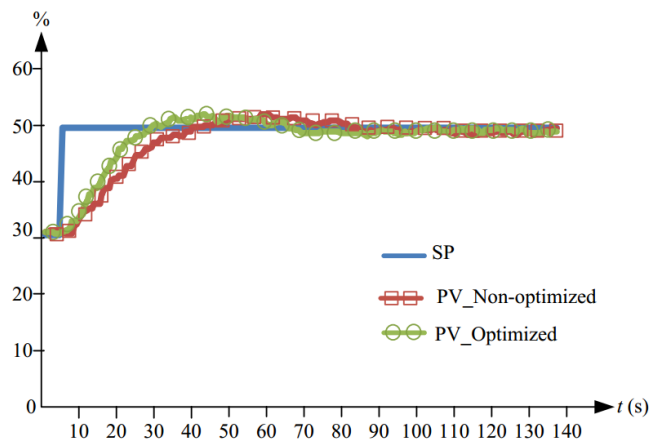
(b) Comparison of Figures 7(a) and 7(b)

FIGURE 8. Step-change responses of the control loop with the macrocycles of Figure 7

From Table 4, it can be seen that the calculated macrocycles of all three cases can be minimized by taking advantage of parallel execution of the function blocks, AI1 and AI2. The network bandwidths available for unscheduled communications are also increased by grouping the scheduled data transmissions to publish the function block outputs on the network. If a lot of time is allocated for unscheduled data transfers, events such as alarm notification, device parameter access, and operator screen update will be fast. In addition, the placement of the primary PID and secondary PID function blocks in the valve positioner of Case 3 provides the minimum network load for scheduled transmission. Optimizing function block links is one of effective methods for optimum communication schedule.

Figure 8(a) shows the responses of the cascade control loop with the optimized macrocycle of Figure 7(b) to step changes of the setpoint. It is evident that the preferred communication schedule can be used to maintain the controlled process within the acceptable operating range. Figure 8(b) displays comparison of two step responses obtained from the control loops with non-optimized and optimized macrocycles of Figure 7. It is seen that the optimized macrocycle with shorter control loop latency offers faster step response.

6. **Conclusions.** A practical technique to optimize segment macrocycles of the FF-based cascade control for better communication and control capabilities has been introduced. The optimization methods for three different cases of control function block allocation are described. Experimental results show that the communication schedules can be improved by scheduling parallel execution of the AI blocks and grouping data transmission for external function block links. Moreover, the system performance can be also improved by reducing the number of external links.

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