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BOOST CIRCUIT DESIGN OF HIGH POWER FACTOR BASED ON THE L6562A

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Abstract. *More and more power electronic technologies are applied to the daily production and life, which provide a new means of control for the power system. And at the same time harmonic pollution is introduced to the grid, which is the main cause of low power factor. With the high demand for power quality in the information age, the harmonic pollution control problem has attracted more and more attention, and the power factor correction technology is also increasingly becoming the focus of research. Power factor correction technology is an effective means to improve the power factor. This paper introduces a boost type of power factor correction circuit based on ST chip L6562A, and the control chip and its peripheral circuit are designed in detail. Stable voltage output and a high power factor are achieved through the circuit simulation and test. The result proves the feasibility of the principle of the circuit.*
Keywords: Power factor correction, Boost circuit, L6562A

1. **Introduction.** Before a lot of power electronic equipment is applied to daily production and life, the main way to control harmonic is to install harmonic compensation equipment [1]. However, with abundant appearance of power electronic devices, simply using compensation device for harmonic compensation has been far from able to solve the problem of harmonic pollution. And researchers begin to transform the converter itself, and make itself not produce harmonic [2]. Compared with compensation device, this approach is more positive, which is now the PFC (power factor correction technology). With further research, PFC has experienced the beginning of passive power factor correction technology to the current APFC (active power factor correction technology) [3].

Since the 90s, many international famous IC companies have produced active PFC control chip circuit, and the APFC technology has made great progress. In recent years, the main circuit of APFC technology has been the advent of new topology. In addition, soft switching technology and more and more control methods are also applied to the power factor correction technology [4,5]. Now a variety of models of commercial control PFC IC are for different converters. Some chips like L6562, MC34262, and UC3852 are suitable for small and medium power applications. Some chips like UC3854A ML4821 are suitable for big power applications [6]. These commercial PFC control chips have a common feature which adopts traditional control strategy. Compared with the same pin package of L6562, L6562A has more excellent performance. L6562A has high linear multiplier which contains patent circuit, can reduce the AC input current distortion, makes the circuit get very low THD in wide input voltage range and a large load changes, and then achieves better power factor correction. At the same time, L6562A has an error amplifier with voltage mode and the precision internal reference voltage, and can

achieve precise control of the output voltage. L6562A has ultra-low start-up current and low quiescent current which can reduce the chip's power consumption, and has the enable/disable function, thereby enhancing the efficiency of the whole circuit, which is easy to meet the energy saving requirements [7].

So this article designs a boost type of power factor correction circuit based on ST chip L6562A, and analyzes the design method of the control chip L6562A peripheral circuit in detail.

2. **The Basic Principle of the Boost Circuit.** The boost circuit topology is shown in Figure 1. In Figure 1, when the switch tube Q switches into conduction, the current I_L flows through the inductor L. Before the inductance coil reaches saturation, current increases linearly, and the electric energy in the form of magnetic energy is stored in the inductor, and then, the capacitance C_{out} discharges and provides energy for the load; When the switch tube Q is turned off, the magnetic energy stored in inductor will change the voltage V_L polarity of the two ends of the inductor L so as to prevent the current I_L from changing suddenly. In this way, the voltage V_L converted by coil L is connected in series with the power source V_{in}, and supplies electricity higher than the output voltage to the capacitor and load. Figure 2 is the relationship diagram of boost circuit voltage and current. In Figure 2, V_{cont} is the control signal of power switch MOSFET, V_I is the voltage of the two ends of MOSFET, and I_D is the current flowing through the diode D. Taking current I_L as a factor to distinguish one another, the working modes of boost circuit can be divided into continuous mode, discontinuous mode and critical mode.

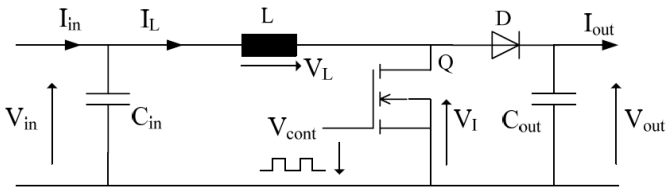

FIGURE 1. Boost circuit topology

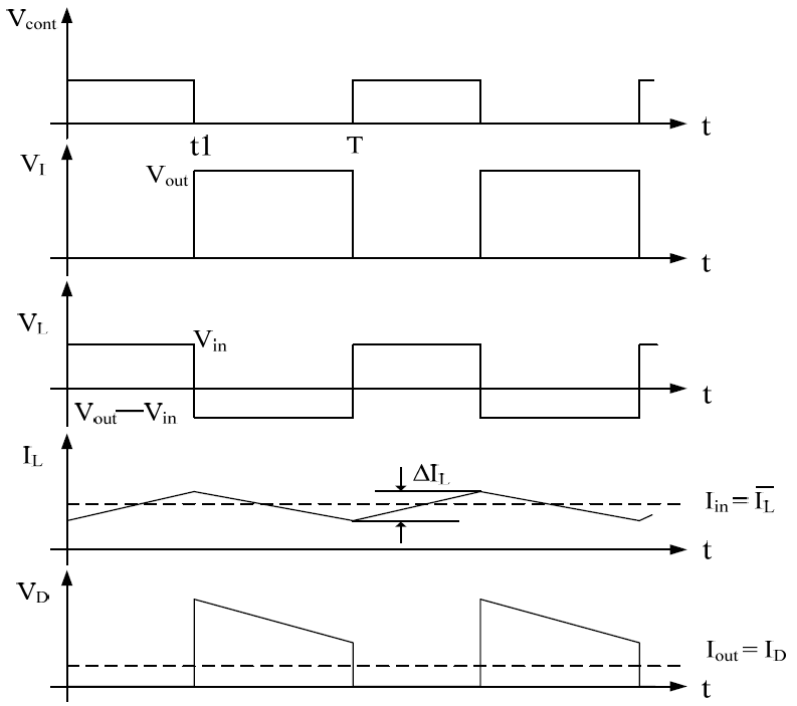

FIGURE 2. Boost circuit voltage and current relationship

By analyzing Figure 2, we can get:

$$\Delta I_L = \frac{i}{L} V_{in} t_2 = \frac{i}{L} (V_{out} - V_{in}) (T - t_2) \tag{1}$$

Then:

$$V_{out} = V_{in} \frac{T}{T - t_2} \tag{2}$$

Type (2) is the basic formula when the boost circuit works in continuous mode and critical mode.

3. The Boost-APFC Circuit Design under the Critical Condition.

3.1. The working principle of PFC critical mode. From Figure 3 we can see that TM (critical conduction mode) mode has a voltage and current dual-loop control structure. Its normal operation control process is as follows.

(1) S conduction stage: The inductance is in the state of charging, and inductor current i_L increases continuously from zero with a fixed slope (V_{in}/L), just like the current curve rise period in Figure 4.

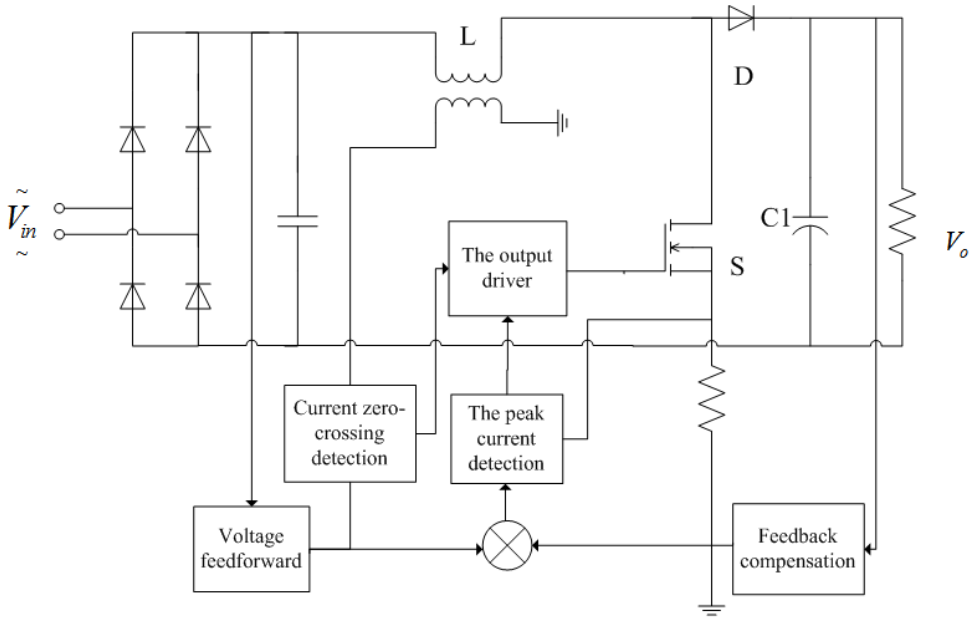

FIGURE 3. TM mode circuit control schematics

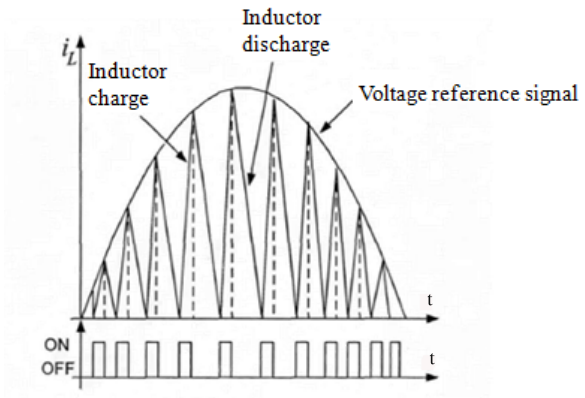

FIGURE 4. Inductor current waveform and driver waveform

(2) S cut-off time: In (1) stage, the peak current detection module compares the voltage obtained from current sampling resistance with the multiplier output signal (the product of voltage feedforward and feedback compensation). When the current value is equal to the multiplier output signal, a signal is sent to turn off the S, and then the inductance enters the stage of discharge.

(3) S cut-off stage: The inductance current begins to drop from the peak with slope $((V_o - V_{in})/L)$, and then the inductance is in the discharge state.

(4) S conduction time: The inductor current is detected from the coupling coil through current zero-crossing detection module. When the inductor current drops to zero (it is generally set to a domain threshold near zero), current zero-crossing detection module will send the ON signal, and controls S conduction through output driver unit. It can be seen in Figure 4. Thereafter the circuit enters (1) stage [8,9].

Critical conduction mode is a kind of variable frequency control, and the switch tube conduction time is constant, but the switch cycle must be changed with the input voltage in order to ensure that the inductor current is always in a critical state. Therefore, this control method is also called the constant on-time control method.

3.2. **Control chip and peripheral circuit design.** Figure 5 as shown below is a power factor correction circuit schematics of power factor output. The circuit operates in critical conduction mode, and it takes the boost type converter circuit as main circuit. The chip belongs to ST company that is PFC circuit control chip L6562A which is specially designed to work in the current critical conduction mode [10,11].

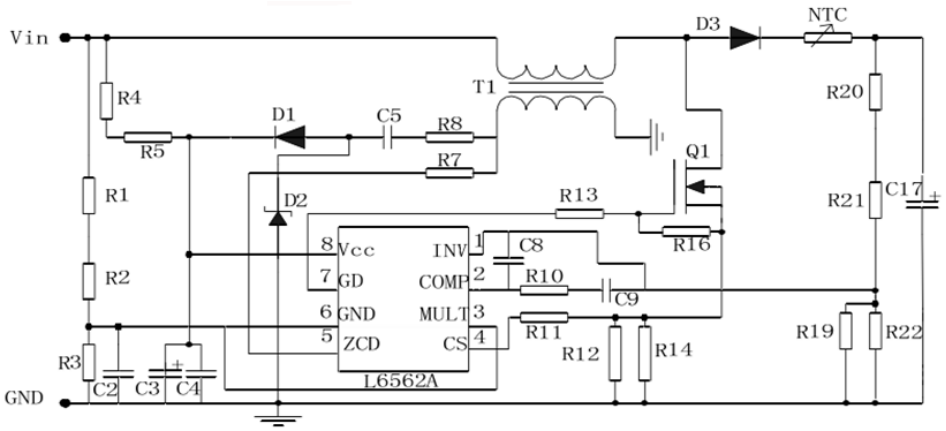

FIGURE 5. TM mode boost PFC circuit schematics

(1) Start-up and power supply circuit design.

As shown above in Figure 5, start-up circuit element comprises R4, R5, C3. In the role of the input pulse voltage, due to the presence of the primary side of the boost inductor, current I_S is induced in the secondary winding, the both ends voltage of boost converter circuit's secondary winding Naux is 14V, the voltage supplies the 8 pins of L6562A with 13V DC voltage when it is rectified and filtered through D1, C3 and C4, to prevent the voltage is too high to damage the chip, and the regulator should be added in the auxiliary winding so as to clamp its output voltage. Because the starting voltage of L6562A is 12.5V, Zener voltage value should be between 12.5V and 22V. The 18V regulator 1N5248B is chosen in design. Fast recovery diode 1N4148 is chosen as D1. R_S, the current limiting resistor, should not be too high; otherwise it will lead to loss and shortage of supplying current for the chip; so 100-ohm resistor can be chosen. C5 plays a role of differential, that is to say, it supplies C3 with power by pulse, and it can also be considered to be a high-impedance; in this way, the power supply of windings is a constant source, so D2 is needed. Start-up resistor R4, R5 should be ensured that they are under the minimum

input voltage V_{in}(min), and provide the IC with adequate large starting current.

$$\mathrm{R4}+\mathrm{R5}<\frac{\sqrt{2}V_{AC(\min)}}{I_{STR(\max)}} \tag{3}$$

R4 is connected in series with R5 in order to constitute the starting resistor, the discharge time of start capacitor should be greater than the time that control chip 8-pin bootstrap voltage reaches the start threshold voltage.

(2) ZCD circuit design.

In the PFC circuit, ZCD pin is connected with boosting inductance auxiliary winding via a current limiting resistor. The trigger mode of ZCD circuit is a negative-going edge trigger, and the trigger will stimulate PWM wave to conduct the MOSFET when ZCD pin voltage is less than 0.7V. Before it drops to 0.7V, pin voltage must be greater than 1.4V, and there is 15% of the left margin. Besides, when power tube is turned off, ZCD pin voltage level is decided by a boosting transformer primary and auxiliary windings ratio, and the maximum boosting transformer primary and auxiliary windings ratio is:

$$n_{\max}=\frac{n_{primary}}{n_{auxiliary}} \tag{4}$$

Manual provisions sink current of ZCD pin should not be greater than 2.5mA, assuming that sink current is $I_{ZCD}=1.35$mA, meanwhile take the boost inductor secondary winding turns as $n_{aux}=6$, and then limiting resistor should meet:

$$\mathrm{R1}\geq\frac{\frac{V_{out}}{n_{aux}}-V_{ZCDH}}{I_{ZCD}} \tag{5}$$

$$\mathrm{R2}\geq\frac{\frac{\sqrt{2}V_{AC(\max)}}{n_{aux}}-V_{ZCDL}}{I_{ZCD}} \tag{6}$$

V_{ZCDH} and V_{ZCDL} are the upper limit and lower limit clamp voltage value of chip ZCD pin, it can be found in chip manual that they are 5.7V and 0V respectively, and here the greater one between R1 and R2 is chosen as limiting resistor.

(3) Design of sense resistor.

Sense resistor R_s is connected to CS pin of the chip, the inverting input of comparator of the chip is connected to the CS pin, noninverting input is connected to the output terminal of the multiplier, what the sensing resistor R_s detects is the inductor current, and then compared with the output voltage of the multiplier; when the voltage across the resistor is equal to the output voltage of the multiplier, there will be trigger signal to turn off the power tube. In order to prevent the main circuit overcurrent condition occurring, chip has overcurrent protection, CS pin clamp voltage $V_{CS\min}$ is 1V, to ensure the normal operation of the circuit, and the sense resistor R_s is to meet:

$$R_s<\frac{V_{CS\min}}{I_{LPK}} \tag{7}$$

The sense resistor power consumption:

$$P_s=I_{sw-rms}^2\cdot R_s \tag{8}$$

(4) The design of multiplier driver resistors.

It can be known from L6562A chip manual that the input voltage range of MULT pin is 0-3V. However, MULT pin gets maximum voltage 3V when the input voltage of PFC circuit reaches maximum.

$$V_{MULT(\max)}=\frac{I_{LPK}\cdot R_s}{1.1}\cdot\frac{V_{AC(\max)}}{V_{AC(\min)}} \tag{9}$$

It can be obtained from the above equation that the maximum value of the resistor divider ratio is:

$$K_P = \frac{V_{MULT(\max)}}{\sqrt{2}V_{AC(\max)}} \tag{10}$$

Dividing resistor is calculated as follows:

$$R_{multH} = \frac{1 - K_P}{K_P} \cdot R_{multL} \tag{11}$$

Then the divider resistor R1, R2 and R3 can be determined.

(5) The bias resistor of error amplifier.

The bias resistor of error amplifier is made up of R20, R21 and R19, R22, which can be used to adjust the output voltage magnitude. The external of chip INV pin is connected to output voltage of PFC which is sampled by the bias resistor of error amplifier, and the internal is connected to inverting input terminal of the error amplifier. The internal of INV pin is connected to DIS circuit, and meanwhile, the overvoltage protection function of the chip will be triggered when DIS current is greater than 27μA. The divider resistor R20, R21 and R19, R22 can be seen in the figure.

$$R_{outH} = \frac{\Delta V_{OVP}}{27\mu\text{A}} \tag{12}$$

$$\frac{R_{outH}}{R_{outL}} = \frac{V_{out}}{2.5\text{V}} - 1 \tag{13}$$

The design requirements can be met if bias resistor is selected reasonably by the formula.

(6) The error amplifier compensation network.

Circuit consisting of capacitors C8, C9 and a resistor R10 has a function of frequency compensation, and the network is positioned between the chip error amplifier inverting input terminal and the output terminal, which can serve to prevent the "missing" low frequency signals and inhibit the function of the output voltage ripple, thereby improving the power factor.

Boost power factor correction circuit compensation network of critical mode is shown as below.

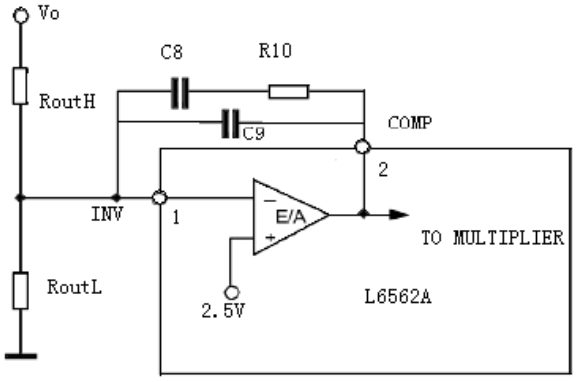

FIGURE 6. PFC compensation network

Hign frequency gain is G_h, and the zero point is Z. Then the feedback capacitance is:

$$\text{C9} = \frac{1}{2\pi \cdot Z \cdot G_h \cdot R_{outH}} \tag{14}$$

The feedback resistance is:

$$\text{R10} = \frac{1}{2\pi \cdot Z \cdot C_S} \tag{15}$$

If it is possible to provide a low-frequency pole and a high DC gain, only one capacitor can be arranged PFC compensation network, assuming the system bandwidth is set to BW, and the compensation capacitor is:

$$C_{comp} = \frac{1}{2\pi \cdot \dfrac{R_{outH} \cdot R_{outL}}{R_{outH} + R_{outL}} \cdot BW} \tag{16}$$

4. **The Circuit Test Results.** Through the analysis and circuit design of the power factor correction circuit working in critical mode, this paper completes the PFC circuit with L6562A as the control chip. Several important waveforms are given below for analyzing when the circuit works.

(1) The inductor current waveform.

Figure 7 shows that the conduction time of the power tube is the time when the inductor current is zero, and the turn-off time is the time when the inductance current is the maximum. Conduction time is constant but the frequency is inconstant, indicating boost converter works in critical conduction mode of the frequency control.

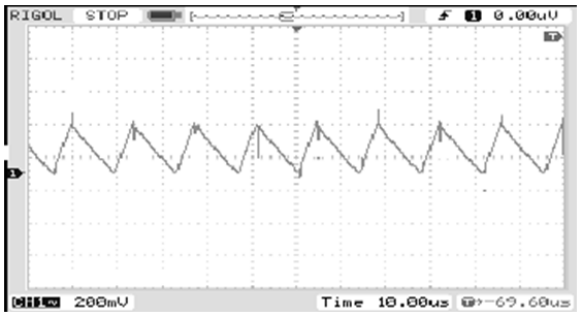

FIGURE 7. The inductor current waveform

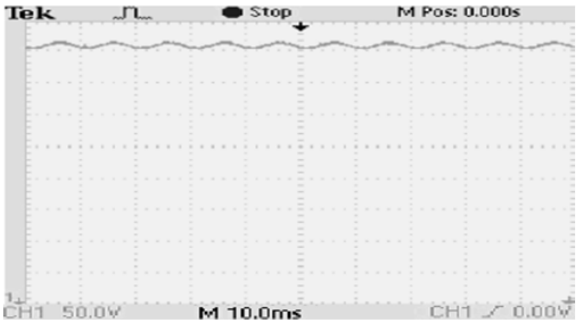

FIGURE 8. Output voltage waveform

FIGURE 9. Output voltage ripple

(2) Output voltage waveform and output voltage ripple.

Above Figure 8 and Figure 9 are respectively output voltage waveform and output voltage ripple, showing that the output voltage is about 400V, and the ripple size is about 10V, which meet the design requirements.

(3) The variation curve of power factor.

In the case of single-phase AC input, the variation curve of PF value with the output power is shown in Figure 10 below.

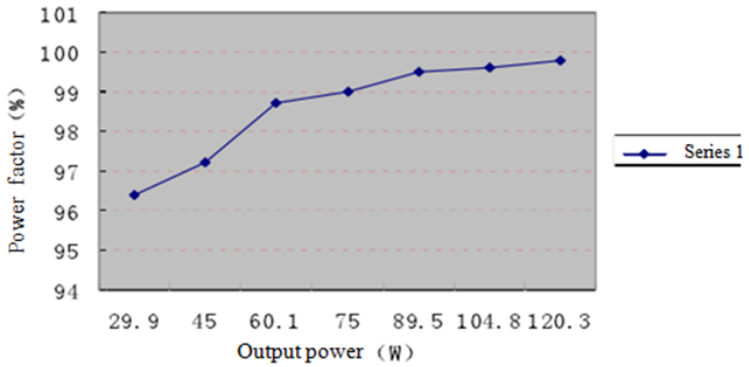

FIGURE 10. The variation curve of PF value with the output power

It can clearly be seen, in the process of load changing from light to heavy, PF value is always above 0.95, and it can reach more than 0.99 in full load.

5. **Conclusions.** In this paper, a boost type power factor correction circuit of high power factor output based on ST chip L6562A is designed. And the focus is the control chip and its peripheral circuits are analyzed and designed in detail. The test proves that the circuit has the advantage of high power factor, good stability, high reliability and so on, which meet the design requirements. However, there are also many imperfect aspects to be studied and many problems to be solved. In the future research, the application of power electronic devices and the design of circuit will be a hot research in eliminating harmonics and improving power factor.

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