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LOW POWER DIVIDER DESIGN USING PASS TRANSISTOR LOGIC CIRCUIT SCHEMES

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Abstract. *In this paper, a novel extended true-single-phase-clock (E-TSPC) based divide-by-3 divider design for low voltage and low power applications is presented. By using pass transistor logic and wire logic circuit techniques, the proposed design is successfully eliminating the extra logic gate between flip-flops. Leading to our design is capable of performing at a higher frequency due to a reduced critical path. Post-layout simulation results show that, compared with conventional design as much as 13.4% in operation speed and 25% in power-delay-product can be achieved by the proposed design. A divide-by-12 divider consisting of the proposed divide-by-3 design and two stages of asynchronous T-FF is developed and implemented in 0.18μm CMOS technology. The measured results show the design is capable of working at 500MHz when the supply voltage is only 0.6V.*
Keywords: Flip-flop, Pass transistor logic, Wire logic, Low voltage, Low power

1. **Introduction.** The high speed divide-by-N divider is a fundamental module for frequency synthesizers because it operates at a higher frequency and consumes higher power consumption [1]. The divide-by-N divider consists of flip-flops (FF) and extra logic to determine the terminal count. For the FF design, the extended true-single-phase-clock (E-TSPC) based FF has been presented for high speed applications [2-4]. Compared to conventional TSPC design [5], the E-TSPC design removes the transistor stacked structure and all the transistors are free of the body effect [6]. The E-TSPC design is thus more sustainable for high operating frequency operations in the face of low voltage supply [7].

The schematic of a conventional E-TSPC based divide-by-3 divider is shown in Figure 1. The states of $Q1b$ and $Q2b$ cycle from 11, 10 to 00 and then return to 11 again for a new cycle. To realize a divide-by-3 divider, two extra logic gates, i.e., an AND gate and an inverter are needed. Past optimization efforts focused mainly on simplifying these logic gates so as to reduce the circuit complexity as well as the critical path delay. For example, the E-TSPC design is embedded with one extra pMOS transistor to form an integrated function of FF and AND logic [2]. This measure, however, leads to an increase in both static and short circuit power due to the ratioed structure in FF designs [4]. In [8], an E-TSPC based pass transistor logic scheme prescaler design is proposed and discussed (simulation results only).

In this paper a novel circuit design technique to tackle both the speed and power issues simultaneously is presented. The AND function is realized in a wired logic fashion at no extra transistor cost. An always turn-on transistor is used to avoid a possible reverse data between the FFs. Performance enhancement is assured by its design simplicity. The rest of the paper is organized as follows. In Section 2, the proposed divide-by-3 divider is explained. In Section 3, post-layout simulation results and experimental results

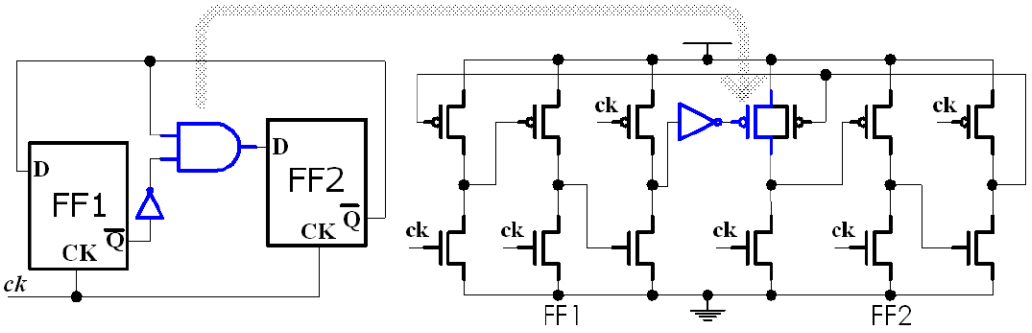


FIGURE 1. Conventional E-TSPC based divide-by-3 divider design

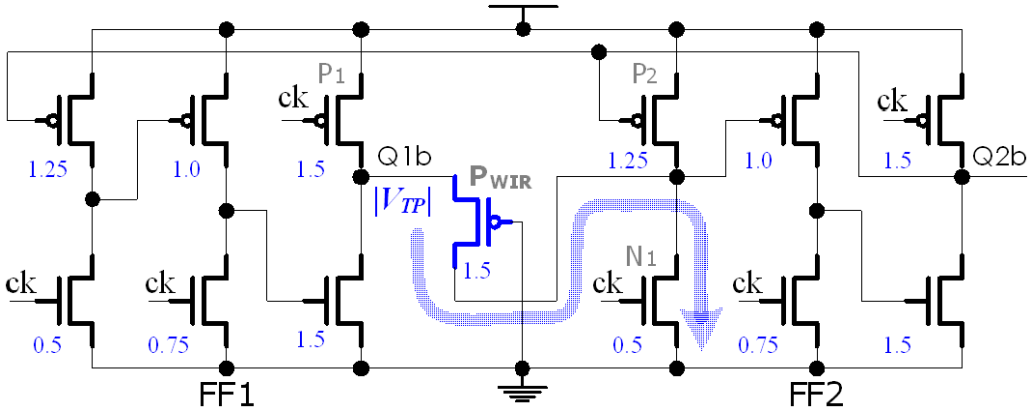


FIGURE 2. Proposed divide-by-3 divider design

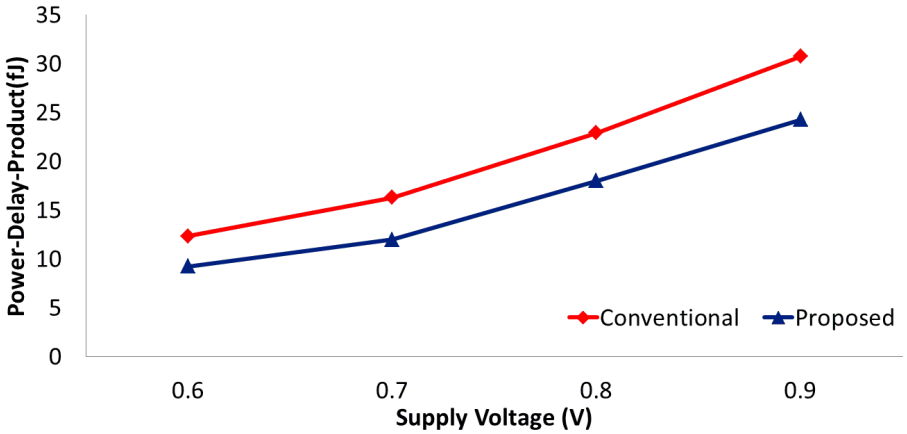
are compiled to demonstrate the superiority of the proposed divider design, and the conclusion is given in Section 4.

2. **Proposed Circuit Design.** The MOS schematic of the proposed E-TSPC based divide-by-3 divider is given in Figure 2. Besides the circuitry of two FFs, only one pMOS transistor P_{WIR} is used. The circuit complexity is greatly reduced, which results in a very compact layout and is beneficial to both operation speed and power consumption factors.

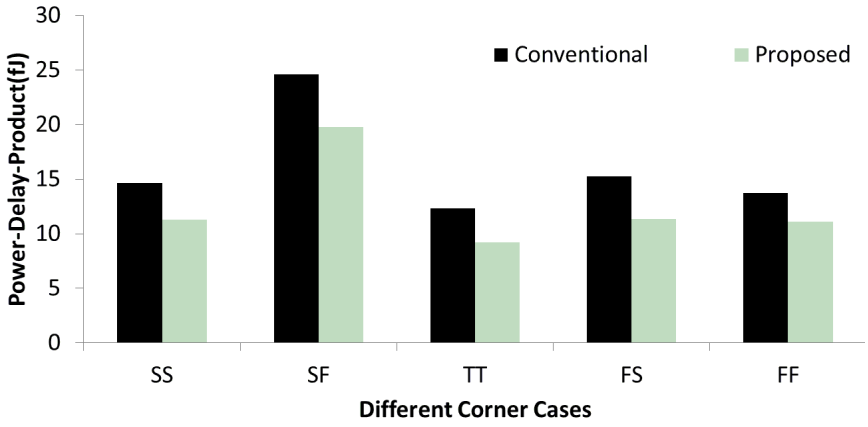
Refer to the MOS schematic shown in Figure 1, previous designs turn the 1st stage inverter of FF2 into a NAND logic and an inverter is needed to convert signal $Q1b$. In our design, signal $Q1b$ is tied, through an always turn-on pMOS transistor, with the output node of the 1st stage inverter of FF2. Either $Q2b$ equal to "0" or $Q1b$ equal to "1" pulls the output node of the inverter high, which is exactly the behavior of NAND logic. In addition, the inverter needed to complement the $Q1b$ signal is no longer needed. The always turn-on pMOS transistor Px, though seeming redundant in logic operation, serves to mitigate the erroneous discharge problem on node $Q1b$ by transistor N1. When $Q1b$ and $Q2b$ are both equal to "1", transistors P_1 and P_2 are off, and node $Q1b$ is supposed to keep the state of FF1 on the parasitic capacitor. Without transistor P_{WIR}, a signal "0" flows backward to destroy the value of $Q1b$ when transistor N1 is turned by the clock signal. An always turn-on pMOS transistor, which is harmless in passing a signal "1" forward, prevents an intact "0" from flowing backward to node $Q1b$. As a result, node $Q1b$ is discharged from V_{DD} to $|V_{TP}|$ only. For low V_{DD} operations, the threshold voltage value is usually larger than one half of the V_{DD}. This value is even higher when taking the body effect into account. The state "1" of $Q1b$ can thus be preserved and the proposed design functions properly, in particular for lower supply voltage operations.

3. **Simulation Results.** Post-layout simulations in HSPICE were conducted to compare the performances between the proposed design and the conventional design shown in Figure 1. The target technology is TSMC 0.18μm CMOS process [9]. Transistor sizing is subject to power-delay-product (PDP) optimization and a typical-size inverter, i.e., 1.5μ/0.5μ was used as the output load.

Figure 3(a) shows the PDP of both designs versus supply voltages less than 1V. The proposed design outperforms the conventional one in all voltage settings. When the supply voltage reaches 0.9V, the PDP saving is 21%. At the same time, the maximum frequencies of our design and the conventional design are 3.02GHz and 2.84GHz, respectively. Figure 3(b) shows the PDP performance of both designs at different process and temperature corners. The voltage is fixed at the lowest V_{DD} 0.6V and the temperature varies from 0°C (FF corner), 25°C (SF, FS and TT corners) to 100°C (SS corner). The performance edge of the proposed design is maintained in all corners.



(a)



(b)

FIGURE 3. PDP performances VS (a) supply voltage (b) process corner

Figure 4 also gives the Monte Carlo simulation results plotted in a scattering diagram using $f_{\max}$ (horizontal) and power (vertical) as the two axes. The control parameters are transistor width and the threshold voltage. It can be clearly seen that the ($f_{\max}$, power) points of the proposed design are located at the lower right corner of the scattering diagram, i.e., higher working speed and lower power consumption. Table 1 summarizes the design features of both divider designs at 0.6V supply voltage. The layout area of the proposed design is 17.7% smaller. The PDP number is also 25% lower. Due to the circuit simplicity, the frequency jitter of the proposed design is also smaller than the conventional

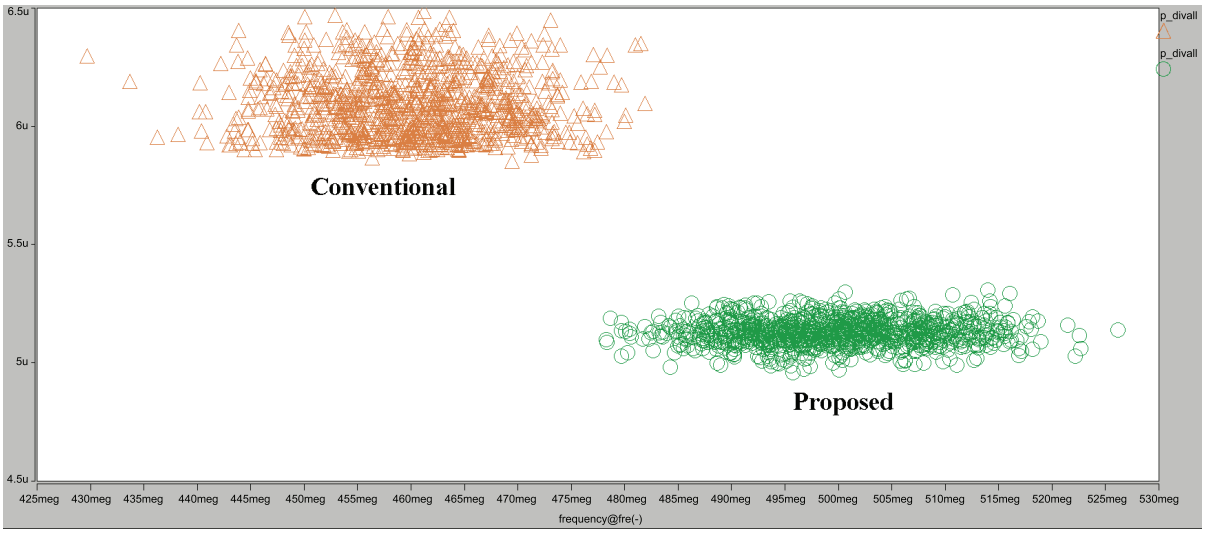


FIGURE 4. Monte Carlo simulation results, power (μW) versus $f_{\max}$ (MHz)

TABLE 1. Simulation results and features (@ TT corner)

Divide-by-3 Divider	Conventional	Proposed
# of Transistor-Count/Area (μm^2)	15/86.08	13/70.87
Max. Frequency (MHz)	484	549
Average Power (μW)	5.96	5.07
Power-Delay-Product (fJ)	12.31	9.23
Jitter (pS)	15.3	8.6

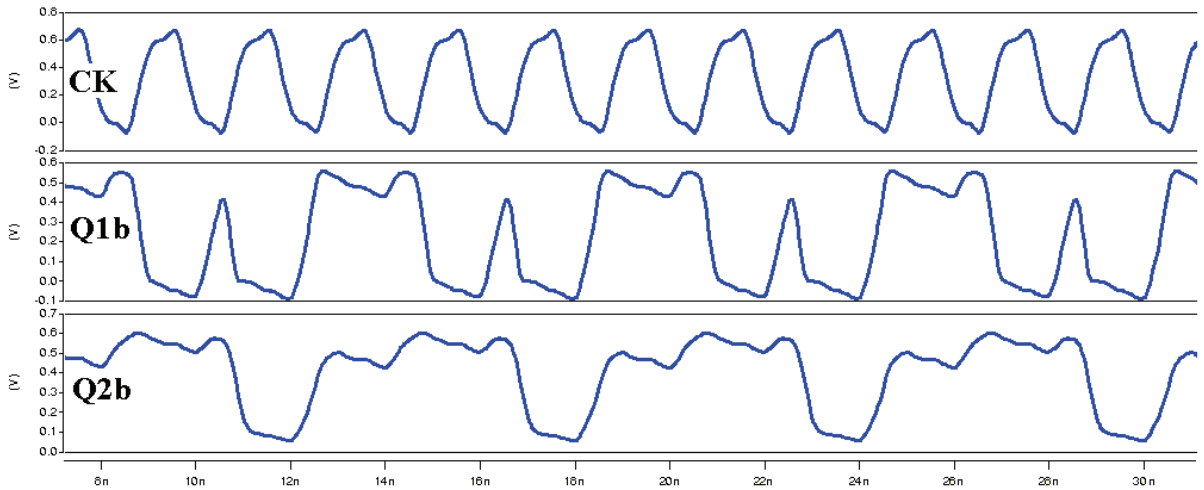


FIGURE 5. Post-layout simulation waveforms of proposed design

design. Numbers for other supply voltages also indicate a consistent performance edge of the proposed design.

Figure 5 depicts the simulation waveforms of the proposed design for 0.6V V_{DD} operations. The waveforms are taken at node $Q2b$ loaded with a typical size inverter. The waveforms show an intact signal "0" and the minimum level of signal "1" is 0.454V, which is large enough to turn off the pull up pMOS transistor in following inverter.

The proposed design is further extended to a divide-by-12 divider design by adding two stages of asynchronous FF (as divide-by-2 each). The extended design is fabricated using

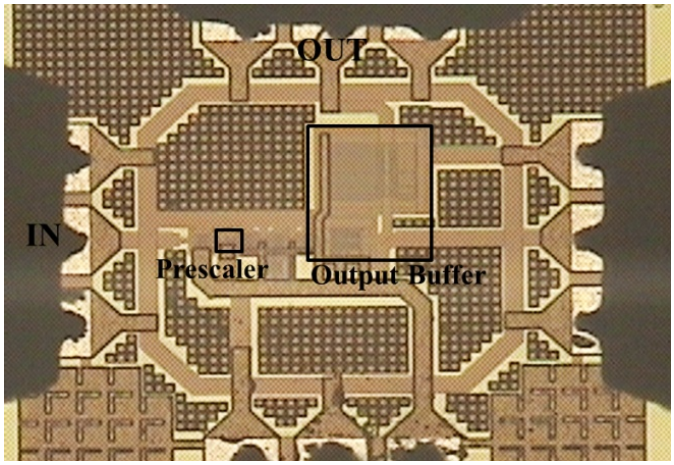


FIGURE 6. Die photo of the divide-by-12 divider design

FIGURE 7. Measured waveforms for the operation of divide-by-12

a TSMC 0.18μm CMOS process. The die photo and the measured waveforms are shown in Figure 6 and Figure 7, respectively. The chip functions correctly at (0.6V/500MHz) and the measured power consumption is 16.75μW. It is expected that the proposed design can be easily migrated to more advanced process technologies. This is because the threshold voltage does not scale proportionally to the V_{DD} scaling and thus provides even better isolation on the reverse signal flow across the P_{WIR} transistor.

4. **Conclusion.** In conclusion, we presented a novel divide-by-3 divider design consisting of E-TSPC FFs plus an embedded wired NAND logic using only one pMOS transistor based on the principle of pass transistor logic. The circuit simplicity leads to short critical path and reduces power consumption. The advantages in power, speed and layout area

against previous design are further verified by post layout simulations. The proposed design is particularly useful for low voltage operations and exhibits significant performance improvements over existing designs. The correct operation of this proposed divider has also been proved. We believe that the proposed circuit technique can be an efficient means for both speed and power in E-TSPC frequency divider circuits.

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