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DESIGN OF AN INDUCTOR-LESS DC-AC INVERTER USING A STEP-DOWN FIBONACCI SEQUENCE GENERATOR

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Abstract. *To supply AC 100V from DC 141V, a step-down Fibonacci DC-AC inverter is proposed in this paper. By using the minimum number of capacitors, the voltage of each capacitor demonstrates the ratio of a stepped-down Fibonacci sequence. By combining these capacitors in series, the proposed inverter offers a modified sinusoidal wave by using smaller number of capacitors than conventional inductor-less inverters. Through simulation program with integrated circuit emphasis (SPICE) simulations, the characteristics of the proposed inverter are clarified.*
Keywords: DC-AC inverters, Inductor-less circuits, Switched-capacitor circuits, Fibonacci numbers, Step-down converters

1. **Introduction.** In small power DC-AC conversion, the demand for a small and light inverter is increasing in recent years. As one of the most promising DC-AC inverters, a switched-capacitor (SC) DC-AC inverter has been attracting much attention, because the SC inverter requires no magnetic component such as transformers and inductors. Due to the inductor-less topology, the SC inverter can achieve not only small size but also low electromagnetic interference (EMI).

To the best of our knowledge, the first SC DC-AC inverter was developed by Marusarz [1] in 1989. Following this, Ueno et al. proposed the novel type DC-AC inverter by connecting SC blocks [2]. In these inverters, a modified sinusoidal wave is offered by boosting an input voltage. By improving Marusarz's inverter, the voltage equational type inverter [3] is suggested by Ishimatsu et al. By converting a DC input, the voltage equational type inverter provides a stepped-down sinusoidal wave. However, the conventional inverters [1-3] are difficult to achieve high power efficiency. Following this, Oota et al. proposed a bidirectional inverter using a series-parallel type converter [4]. To achieve high power efficiency and small ripple noise, the bidirectional inverter [4] is synthesized by connecting series-parallel type converters in parallel. On the other hand, Terada et al. suggested a programmable inverter using a ring type converter [5]. By changing a pattern of clock pulses, the programmable inverter [5] can offer flexible conversion ratios. However, the conventional inverters in [1-5] require many circuit components, because the step-up/step-down gain is proportional to the number of transfer capacitors. To achieve small number of circuit components and high step-up/step-down gain, Chang suggested the multistage switched-capacitor-voltage-multiplier (SCVM) DC-AC inverter [6]. By connecting boost converters in series, the SCVM can achieve high gain. However, many circuit components are still necessary, because the voltage ratio of all transfer capacitors is the same. To overcome this problem, a multistage multiphase (MSMP) boost DC-AC inverter [7] was

proposed by Chang. By using multiphase pulses, the MSMP boost inverter can achieve the 2^N $(N = 2, 3, \ldots)$ step-up gain. However, the MSMP boost inverter provides the output voltage only once every $N + 1$ phases. Therefore, the power efficiency of the MSMP boost inverter is low. On the other hand, we proposed a step-up Fibonacci SC DC-AC inverter [8,9]. In the step-up Fibonacci inverter, each capacitor is charged to the voltage of the preceding stage and then stepped-up by the voltage of the preceding stage increasing the voltage of the next stage. By iterating these two processes, the voltage ratio of transfer capacitors becomes a Fibonacci number. Therefore, the step-up Fibonacci inverter achieves higher step-up gain and smaller number of circuit components than the SCVM DC/AC inverter. However, the conventional inverters [7-9] cannot offer a stepped-down AC output by converting a DC input.

In this paper, a step-down Fibonacci DC-AC inverter is proposed in order to supply AC 100V from DC 141V. By using the minimum number of capacitors, the voltage of each capacitor demonstrates the ratio of a stepped-down Fibonacci sequence. By combining these capacitors in series, the proposed inverter offers a modified sinusoidal wave by using smaller number of capacitors than conventional inductor-less inverters. To show the effectiveness of the proposed inverter, theoretical analysis and simulation program with integrated circuit emphasis (SPICE) simulations are performed.

The rest of this paper is organized as follows. In Section 2, the circuit configuration of the step-down SC inverters is presented. In Section 3, the characteristic of the proposed inverter is clarified by SPICE simulation. Finally, conclusion and future work are drawn in Section 4.

2. **Circuit Configuration.**

2.1. **Conventional step-down inverter.** As a conventional SC inverter, the step-down SC inverter [3] is described in this subsection, because other conventional SC inverters [1,2,4-9] are difficult to achieve step-down conversion. Figure 1 illustrates the circuit configuration of the conventional step-down SC inverter [3]. In Figure 1, the transistor switches are controlled by non-overlapped N $(= 2, 3, \ldots)$-phase pulses as shown in Figure 1. By using the flying capacitor C_0, the voltage of each capacitor becomes

$$V_{Ck} = \frac{V_{in}}{N} \quad (k = 1, 2, \ldots, N). \tag{1}$$

Therefore, by controlling S_{ok} in Figure 1, the converter block offers the following conversion ratios:

$$V_o = \left\{ \frac{1}{N}, \frac{2}{N}, \frac{3}{N}, \cdots, \frac{N-1}{N}, \frac{N}{N} \right\} \times V_{in}. \tag{2}$$

The full bridge circuit reverts the polarity of V_o alternately at every cycle to output AC voltage V_{out}.

2.2. **Proposed inverter.** Figure 2 illustrates the circuit configuration of the proposed inverter. Unlike the conventional inverter of Figure 1, the transistor switches of the proposed inverter are controlled by non-overlapped four-phase pulses as shown in Table 1. In Table 1, State-T_1 and T_3 are charging periods. On the other hand, State-T_2 and T_4 are transferring periods. In the proposed inverter, each capacitor is charged to satisfy the following conditions:

$$V_{Ci} = \sum_{j=i+1}^{i+2} V_{Cj} \quad (i = 0, 1, 2, \ldots, N), \tag{3}$$

where $V_{C0} = V_{in}$ and $V_{Cj} = 0$ if $j > N$.

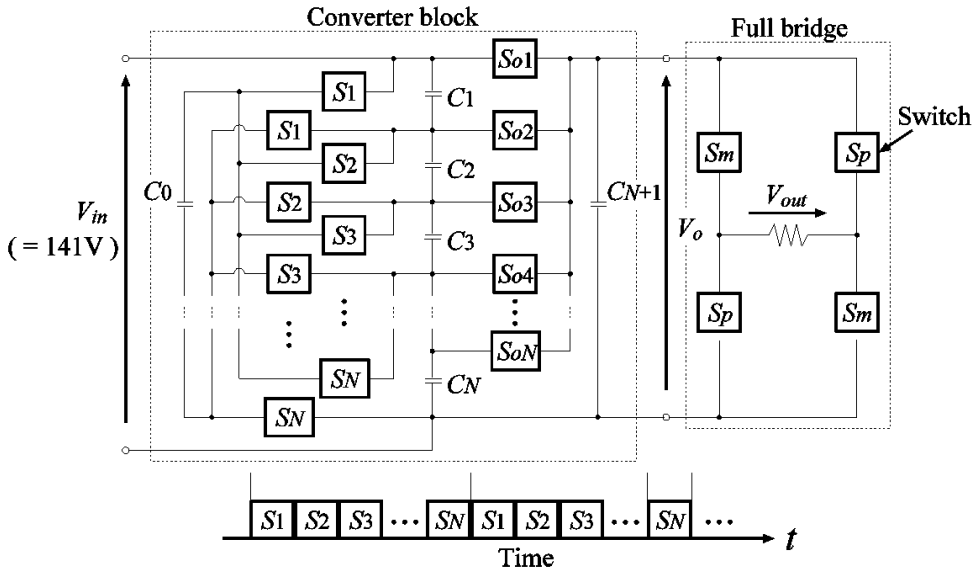

FIGURE 1. Circuit configuration of the conventional step-down SC inverter [3]

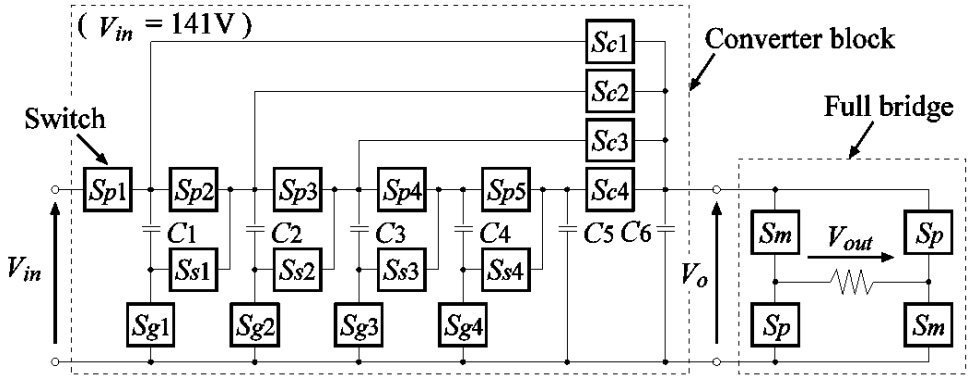

FIGURE 2. Circuit configuration of the proposed inverter

TABLE 1. Timing of clock pulses

Ratio	State	On Switch	Off Switch
$\frac{1}{8}\times, \ldots, \frac{8}{8}\times$	T_1	S_{p1}, S_{s1}, S_{g2}, S_{p3}, S_{s3}, S_{g4}, S_{p5}	Other switches
	T_3	S_{g1}, S_{p2}, S_{s2}, S_{g3}, S_{p4}, S_{g4}, S_{s4}	Other switches
$\frac{1}{8}\times$	T_2 and T_4	S_{g4}, S_{p5}, S_{c4}	Other switches
$\frac{2}{8}\times$	T_2 and T_4	S_{g3}, S_{c3}	Other switches
$\frac{3}{8}\times$	T_2 and T_4	S_{g2}, S_{c2}	Other switches
$\frac{4}{8}\times$	T_2 and T_4	S_{g4}, S_{p4}, S_{s2}, S_{c2}	Other switches
$\frac{5}{8}\times$	T_2 and T_4	S_{g1}, S_{c1}	Other switches
$\frac{6}{8}\times$	T_2 and T_4	S_{g4}, S_{p3}, S_{p4}, S_{s1}, S_{c1}	Other switches
$\frac{7}{8}\times$	T_2 and T_4	S_{g3}, S_{p3}, S_{s1}, S_{c1}	Other switches
$\frac{8}{8}\times$	T_2 and T_4	S_{p1}, S_{c1}	Other switches

From (3), the voltage ratio of the capacitors, V_{Ci}'s, becomes the ratio of the Fibonacci sequence. Concretely, the voltage ratio of capacitors is as follows:

$$C_1 : C_2 : C_3 : C_4 : C_5 : V_{in} = \frac{1}{8} : \frac{1}{8} : \frac{2}{8} : \frac{3}{8} : \frac{5}{8} : \frac{8}{8}. \tag{4}$$

In State-T_2 and T_4, the proposed inverter offers a modified sinusoidal wave by combining these capacitors in series. Table 2 shows the comparison of circuit components between the proposed inverter and the conventional inverter of Figure 1. As you can see from Table 2, the proposed inverter can reduce 4 capacitors and 7 switches from the conventional inverter.

TABLE 2. Comparison of the number of circuit components

	Number of capacitors	Number of switches
Proposed Inverter	6	21
Conventional Inverter [3]	10	28

3. **Simulation.** To clarify the characteristics of the proposed inverter, SPICE simulations are performed under conditions that $V_{in} = 141$V, $C_1 = \ldots = C_5 = 33\mu$F, $C_6 = 3.3\mu$F, and $T_s = 0.5\mu$s. Figure 3 demonstrates the simulated output voltage when the output load is 10kΩ. As you can see from Figure 3, the proposed inverter can provide a modified sinusoidal wave. Figure 4 shows the simulated power efficiency as a function of the output load. The proposed inverter can realize more than 90% power efficiency in the range of 40 to 840W. As Figure 4 shows, the proposed inverter can achieve higher power efficiency than the conventional step-down SC inverter. Concretely, about 3% power efficiency is

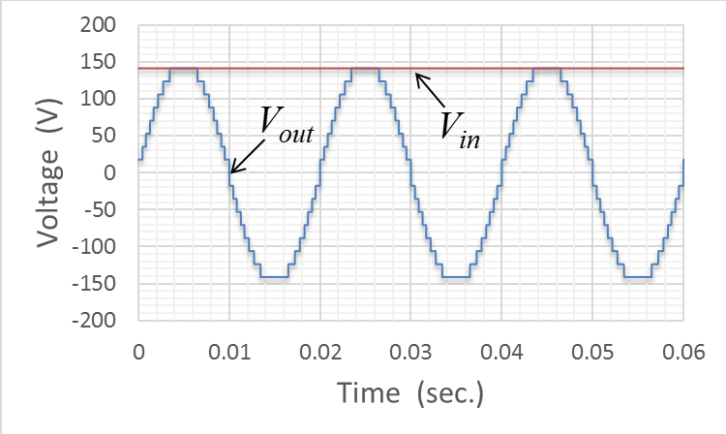

FIGURE 3. Simulated output waveform

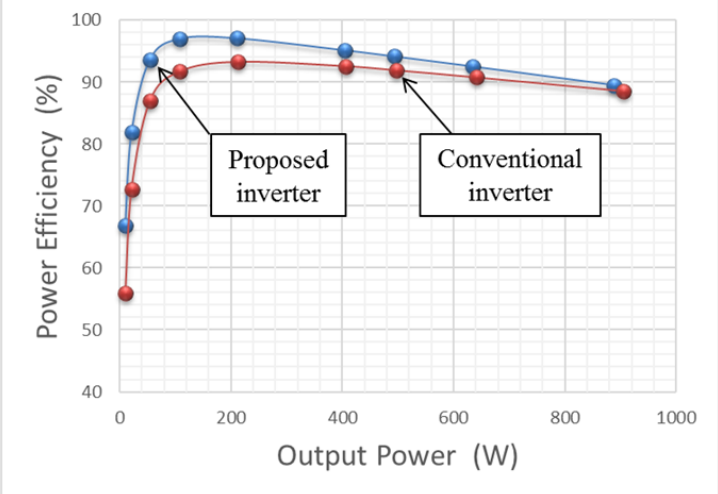

FIGURE 4. Simulated power efficiency as a function of the output load

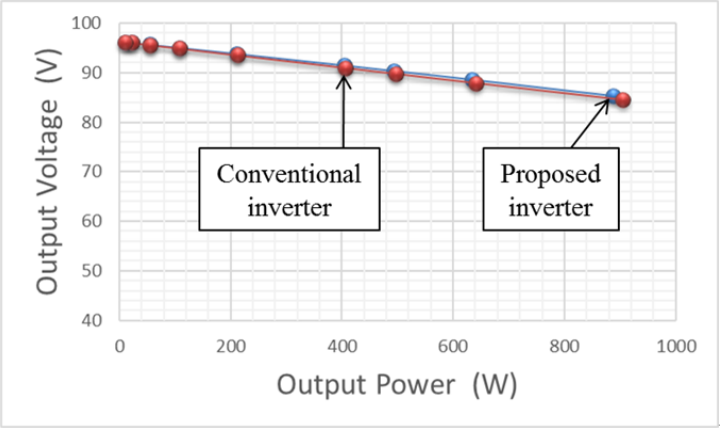

FIGURE 5. Simulated output voltage as a function of the output load

improved by the proposed inverter when the output power is 400W. Figure 5 shows the simulated output voltage as a function of the output load. The proposed inverter can achieve about 90% voltage efficiency when the output power is less than 520W. From these results, the proposed inverter can realize not only small size but also high power efficiency.

4. **Conclusions.** A step-down Fibonacci DC-AC inverter is proposed in order to supply AC 100V from DC 141V. Concerning the output voltage and power efficiency, SPICE simulations were performed to clarify the characteristics of the proposed inverter.

The number of circuit components for the proposed inverter is less than that for the conventional step-down SC inverter. Concretely, 4 capacitors and 7 switches are reduced from the conventional step-down SC inverter. Therefore, the proposed inverter can achieve small volume and light weight. The result of the SPICE simulations showed that the proposed inverter can achieve higher power efficiency. The proposed inverter improved 3% power efficiency from the conventional step-down SC inverter when the output power is 400W.

To confirm the validity of circuit design, the experiment and theoretical analysis are left to a future study.

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