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DIGITAL-DOMAIN SELF-CALIBRATION OF CAPACITOR MISMATCH FOR SAR ADC WITHOUT ADDITIONAL CALIBRATION DAC

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Abstract. *A digital-domain self-calibration technique that calibrates capacitor mismatch of digital-to-analog converter (DAC) for successive approximation register (SAR) analog-to-digital converter (ADC) is presented. An extra calibration DAC is not required, because the error voltages due to the mismatches in the most-significant-bit (MSB) side part of DAC can be measured by the least-significant-bit (LSB) side part of DAC. Moreover, the terminal capacitors combined with a third reference voltage are used to further improve the calibration precision. A 12-bit SAR ADC is implemented in 40nm CMOS technology to verify the proposed calibration technique. The simulation result shows that the proposed calibration technique can significantly improve the performance of SAR ADC.*

Keywords: Successive approximation register (SAR), Analog-to-digital converter (ADC), Self-calibration, Capacitor mismatch

1. **Introduction.** Capacitor mismatch of digital-to-analog converter (DAC) seriously limits the linearity of charge redistribution successive approximation register (SAR) analog-to-digital converter (ADC). Usually, larger capacitors can be applied to meeting the requirement of match performance. However, the larger capacitors not only increase the area and power consumption of SAR ADC, but also increase the settlement time of DAC. Recently, several calibration techniques have been proposed to improve the capacitor match performance [1-6]. Thus, the smaller capacitors can be applied to decreasing the area and power consumption of SAR ADC. However, those calibration techniques reported in [1,2] require massive computation. The techniques in [3,4] require an additional reference ADC and an additional calibration DAC, respectively, resulting in increasing chip area and power consumption. The method in [5] works as a single-ended circuit and needs an FIR LPF to reduce the effect of the common-mode noise. The SDEC method [6] is designed for single-ended SAR ADC and not suitable for fully differential one.

In this paper, a digital-domain self-calibration technique without extra calibration DAC and extensive computation is presented and verified by simulation. Moreover, the calibration precision is further improved by using the terminal capacitors combined with a third reference voltage to generate an additional redundant bit for calibration. The simulation result shows that the signal to noise and distortion ratio (SNDR) and the spurious free dynamic range (SFDR) are improved from 58.2 to 71.1dB and 64 to 78.2dB, respectively, for a 12-bit fully differential binary-weighted SAR ADC.

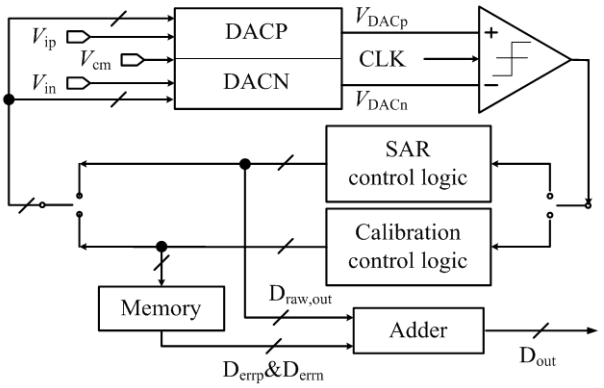
The remainder of this paper is organized as follows. Section 2 introduces the architecture of SAR ADC with proposed calibration technique. Section 3 illustrates the detailed

implementation of the proposed digital-domain self-calibration technique. The application example of SAR ADC with digital calibration technique and simulation results are presented in Section 4 and conclusions are made in Section 5.

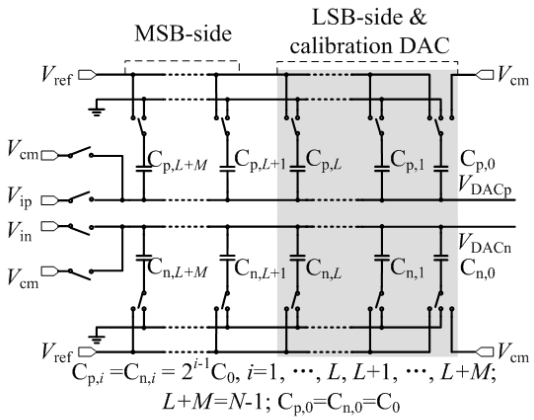
2. **The Architecture of SAR ADC with Proposed Calibration Technique.** Figure 1(a) shows the proposed N-bit SAR ADC with self-calibration, which consists of two differential DAC branches (DACP, DACN), comparator, SAR control logic, calibration control logic, memory and adder. The schematic of the differential DAC is shown in Figure 1(b) and the DAC can be regarded as two parts: MSB-side part (non-shaded part) and LSB-side part (shaded part). The MSB-side part consists of M-bit capacitor array. The LSB-side part consists of L-bit capacitor array and a pair of unit capacitor ($C_{p,0}$ and $C_{n,0}$). N is the sum of L, M and 1.

After powered on, SAR ADC first jumped into the getting error code (GEC) phase. During this phase, DAC, comparator and the calibration control logic constitute a measurement loop. The voltage of V_{cm} is sampled on both DACP and DACN, and the LSB-side part in DAC is used as a calibration DAC to measure the error voltage of each bit due to the capacitor mismatch in the MSB-side part. Then these corresponding error voltages are digitized into error codes and these error codes are stored in the memory.

After the GEC phase, the SAR ADC goes into the normal conversion (NC) phase. The normal conversion loop consists of DAC, comparator and the SAR control logic. The input voltages V_{ip} and V_{in} are sampled on DACP and DACN, respectively. Benefited



(a)



(b)

FIGURE 1. (a) Block diagram of the proposed N-bit fully differential SAR ADC architecture with self-calibration; (b) the schematic of the differential DAC

from the top-plate sampling, the MSB-side part can be used to generate higher M+1-bit digital codes $(\mathrm{D}_{L+M},\ldots,\mathrm{D}_{L+1},\mathrm{D}_L)$. During the normal conversion phase, the LSB-side part is reused to generate lower L-bit and a redundant bit codes $(\mathrm{D}_{L-1},\ldots,\mathrm{D}_0,\mathrm{D}_{0.5})$. The additional redundant bit $(\mathrm{D}_{0.5})$ is generated by the terminal capacitors ($\mathrm{C}_{\mathrm{p},0}$ and $\mathrm{C}_{\mathrm{n},0}$) combined with the voltage of V_{cm} ($V_{\mathrm{cm}} = 1/2\mathrm{V}_{\mathrm{ref}}$). It is only used for calibration with a weighted factor of 0.5LSB.

3. **The Implementation of Proposed Digital-Domain Self-Calibration Technique.**

3.1. **Principle.** During the normal conversion phase, the output voltage of DACN (V_{DACn}) gradually approaches as follows

$$\begin{aligned} & V_{\mathrm{DACn}} \\ = \; & V_{\mathrm{in}} + \left[\frac{V_{\mathrm{ref}}}{2^{L+M}}\left(2^{L+M-1}\mathrm{D}_{L+M}+\cdots+2^{L}\mathrm{D}_{L+1}+2^{L-1}\mathrm{D}_L+\cdots+\mathrm{D}_1+0.5\mathrm{D}_0\right)\right] \\ & + \left[V_{\mathrm{errn},L+M}\mathrm{D}_{L+M}+\cdots+V_{\mathrm{errn},L+1}\mathrm{D}_{L+1}+V_{\mathrm{errn},L}\mathrm{D}_L+\cdots+V_{\mathrm{errn},1}\mathrm{D}_1+V_{\mathrm{errn},0}\mathrm{D}_0\right] \end{aligned} \tag{1}$$

where $V_{\mathrm{errn},i}$ $(i=0,\ldots,L,\ldots,L+M)$ is the error voltage due to the mismatch of capacitor $\mathrm{C}_{\mathrm{n},i}$ in DACN. Assuming that the mismatch of the unit capacitor C_0 has a zero mean and a standard deviation of σ_0, and the mismatches of all the capacitors are independent identically distributed random variables. Then the variation of the mismatch value $\Delta\mathrm{C}_{\mathrm{n},i}$ of capacitor $\mathrm{C}_{\mathrm{n},i}$ $(i=1,\ldots,L,\ldots,L+M)$ in DACN can be derived as

$$\mathrm{E}\left(\Delta\mathrm{C}_{\mathrm{n},i}^2\right) = 2^{i-1}\sigma_0^2, \quad i=1,\ldots,L,\ldots,L+M \tag{2}$$

So, the variation of the error voltage $V_{\mathrm{errn},i}$ can be obtained as

$$\mathrm{E}(V_{\mathrm{errn},i}^2) = \mathrm{E}\left(\frac{\Delta\mathrm{C}_{\mathrm{n},i}^2}{\mathrm{C}_{\mathrm{n,total}}^2}V_{\mathrm{ref}}^2\right) = 2^{i-1}\frac{\sigma_0^2}{\mathrm{C}_0^2}\frac{V_{\mathrm{ref}}^2}{2^{2(L+M)}}, \quad i=1,\ldots,L,\ldots,L+M \tag{3}$$

where $\mathrm{C}_{\mathrm{n,total}}$ is the total capacitance in DACN. This analysis method can also be used for DACP, so the output voltage of DACP (V_{DACp}) is derived as follows, by substituting D_i into $(1-\mathrm{D}_i)$ in (1)

$$\begin{aligned} & V_{\mathrm{DACp}} \\ = \; & V_{\mathrm{ip}} + V_{\mathrm{ref}} - \left[\frac{V_{\mathrm{ref}}}{2^{L+M}}\left(2^{L+M-1}\mathrm{D}_{L+M}+\cdots+2^{L}\mathrm{D}_{L+1}+2^{L-1}\mathrm{D}_L+\cdots+\mathrm{D}_1+0.5\mathrm{D}_0\right)\right] \\ & - \left[V_{\mathrm{errp},L+M}\mathrm{D}_{L+M}+\cdots+V_{\mathrm{errp},L+1}\mathrm{D}_{L+1}+V_{\mathrm{errp},L}\mathrm{D}_L+\cdots+V_{\mathrm{errp},1}\mathrm{D}_1+V_{\mathrm{errp},0}\mathrm{D}_0\right] \end{aligned} \tag{4}$$

The variation of the error voltage ($V_{\mathrm{errp},i}$) due to the mismatch of capacitor $\mathrm{C}_{\mathrm{p},i}$ in DACP can also be achieved as

$$\mathrm{E}\left(V_{\mathrm{errp},i}^2\right) = 2^{i-1}\frac{\sigma_0^2}{\mathrm{C}_0^2}\frac{V_{\mathrm{ref}}^2}{2^{2(L+M)}}, \quad i=1,\ldots,L,\ldots,L+M \tag{5}$$

According to (3) and (5), the linearity of capacitive DAC is mainly determined by the match performance of the MSB-side part of DAC. If the maxim standard deviation of the total error voltages due to the mismatches in the LSB-side part of DAC is smaller than 0.5LSB by 3σ, as

$$3\sigma_{L,\max} = 3\sqrt{\sum_{i=0}^{L}\left[\mathrm{E}\left(V_{\mathrm{errp},i}^2\right)+\mathrm{E}\left(V_{\mathrm{errn},i}^2\right)\right]} = 3\sqrt{2^{L+1}}\frac{\sigma_0}{C_0}\mathrm{LSB} < 0.5\mathrm{LSB} \tag{6}$$

then the mismatches in the LSB-side part of DAC can be neglected. Thus, the LSB-side part of DAC can be reused as a calibration DAC to measure the capacitor mismatch of each bit in the MSB-side part of DAC.

The error voltages ($V_{\mathrm{errp},i}$ and $V_{\mathrm{errn},i}$, $i = L+1,\ldots,L+M$) due to the mismatch of capacitor $\mathrm{C_{p,}}_i$ and $\mathrm{C_{n,}}_i$ in the MSB-side part of DAC can be converted to the digital codes ($\mathrm{D_{errp,}}_i$ and $\mathrm{D_{errn,}}_i$, $i = L+1,\ldots,L+M$) with a weight factor of $V_{\mathrm{ref}}/2^{L+M}$. Hence, the input voltage can be expressed as

$$\begin{aligned} & V_{\mathrm{ip}} - V_{\mathrm{in}} \\ = & \frac{V_{\mathrm{ref}}}{2^{L+M}}\left(2^{L+M}\mathrm{D}_{L+M} + \cdots + 2^{L+1}\mathrm{D}_{L+1} + \cdots + 2^{1}\mathrm{D}_{1} + \mathrm{D}_{0}\right) - V_{\mathrm{ref}} \\ & + \left(V_{\mathrm{errp},L+M} + V_{\mathrm{errn},L+M}\right)\mathrm{D}_{L+M} + \cdots + \left(V_{\mathrm{errp},L+1} + V_{\mathrm{errn},L+1}\right)\mathrm{D}_{L+1} \\ = & \frac{V_{\mathrm{ref}}}{2^{L+M}}\left(2^{L+M}\mathrm{D}_{L+M} + \cdots + 2^{L+1}\mathrm{D}_{L+1} + \cdots + 2^{1}\mathrm{D}_{1} + \mathrm{D}_{0}\right) - V_{\mathrm{ref}} \\ & + \frac{V_{\mathrm{ref}}}{2^{L+M}}\left(\mathrm{D}_{\mathrm{errp},L+M} + \mathrm{D}_{\mathrm{errn},L+M}\right)\mathrm{D}_{L+M} + \cdots + \frac{V_{\mathrm{ref}}}{2^{L+M}}\left(\mathrm{D}_{\mathrm{errp},L+1} + \mathrm{D}_{\mathrm{errn},L+1}\right)\mathrm{D}_{L+1} \end{aligned} \tag{7}$$

Thus, the corrected output code $\mathrm{D_{out}}$ of SAR ADC after calibration can be expressed as

$$\begin{aligned} \mathrm{D_{out}} &= \frac{2^{L+M}}{V_{\mathrm{ref}}}\left(V_{\mathrm{ip}} - V_{\mathrm{in}} + V_{\mathrm{ref}}\right) \\ &= \left(2^{L+M}\mathrm{D}_{L+M} + \cdots + 2^{L+1}\mathrm{D}_{L+1} + \cdots + 2^{1}\mathrm{D}_{1} + \mathrm{D}_{0}\right) \\ &\quad + \left(\mathrm{D}_{\mathrm{errp},L+M} + \mathrm{D}_{\mathrm{errn},L+M}\right)\mathrm{D}_{L+M} + \cdots + \left(\mathrm{D}_{\mathrm{errp},L+1} + \mathrm{D}_{\mathrm{errn},L+1}\right)\mathrm{D}_{L+1} \end{aligned} \tag{8}$$

3.2. **Error-code estimation of capacitor mismatch.** During the GEC phase, the error voltages $V_{\mathrm{errn},i}$ and $V_{\mathrm{errp},i}$ ($i = L+1,\ldots,L+M$) are converted to $(L+2)$-bit digital codes $\mathrm{D_{errn,}}_i$ and $\mathrm{D_{errp,}}_i$, respectively. The error estimation procedure includes three phases, i.e., pre-charge phase, switching phase and estimation phase. After the pre-charge phase and the switching phase, the error voltages are achieved at the output node of DAC. Then during the estimation phase, the error voltages are digitized into error codes. The details of these phases are described as below.

The error estimation procedure of $V_{\mathrm{errp},L+M}$ will be described as an example. During the pre-charge phase, the top plates of all capacitors in DAC are connected to V_{cm}. The bottom plates of the capacitor $\mathrm{C_{p,}}_{L+M}$ of DACP and all capacitors of DACN are discharged to GND; the rest of DACP are pre-charged to V_{ref} as shown in Figure 2(a). During the switching phase, the top plates of all capacitors in DAC are disconnected to V_{cm}. The bottom plate of the capacitor $\mathrm{C_{p,}}_{L+M}$ of DACP is switched to V_{ref} and the rest of DACP are switched to GND as shown in Figure 2(b). Then the output voltage (V_{DAC}) of the

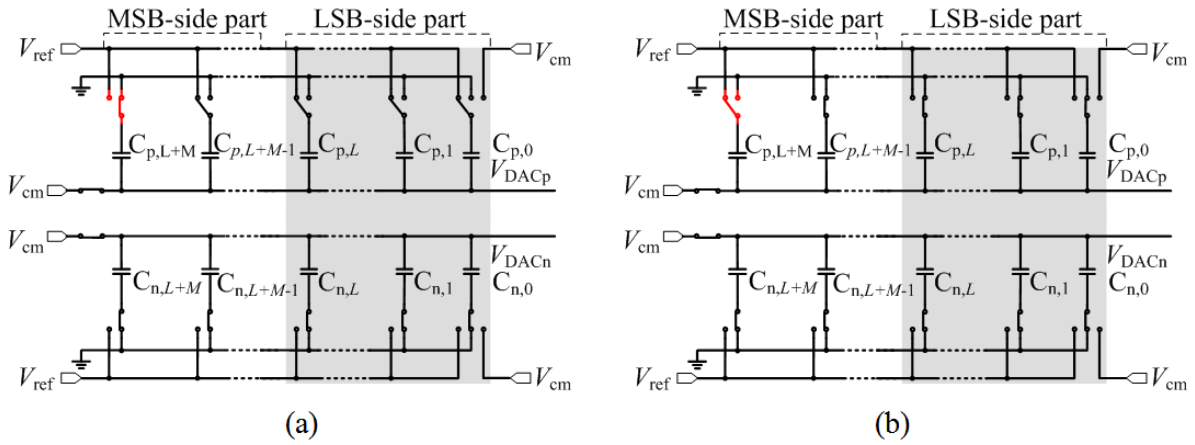


FIGURE 2. (a) Pre-charge phase of the error estimation procedure of $V_{\mathrm{errp},L+M}$; (b) switching phase of the error estimation procedure of $V_{\mathrm{errp},L+M}$

DAC is achieved as

$$\begin{aligned} V_{\mathrm{DAC}} &= V_{\mathrm{DACp}} - V_{\mathrm{DACn}} = V_{\mathrm{cm}} + \frac{V_{\mathrm{ref}}}{2^{L+M}} 2^{L+M\text{-}1} + V_{\mathrm{errp},L+M} \\ &\quad - \frac{V_{\mathrm{ref}}}{2^{L+M}} \left(2^{L+M-2} + \cdots + 1 + 1\right) - \left(V_{\mathrm{errp},L+M-1} + \cdots + V_{\mathrm{errp},0}\right) - V_{\mathrm{cm}} \\ &= V_{\mathrm{errp},L+M} - \left(V_{\mathrm{errp},L+M-1} + \cdots + V_{\mathrm{errp},0}\right) = 2V_{\mathrm{errp},L+M-1} \end{aligned} \tag{9}$$

In Equation (9), it is the fact that the summation of all error voltages ($V_{\mathrm{errp},L+M} + V_{\mathrm{errp},L+M-1} + \cdots + V_{\mathrm{errp},0} = 0$) is zero. After the switching phase, the error voltage of $V_{\mathrm{errp},N-1}$ due to the mismatch of capacitor $\mathrm{C}_{\mathrm{p},L+M}$ in the DACP is achieved. During the estimation phase, this error voltage of $V_{\mathrm{errp},L+M}$ is converted to $(L+2)$-bit digital code $\mathrm{D}_{\mathrm{errp},L+M}$ of $(\mathrm{D}_{\mathrm{E},L}, \ldots, \mathrm{D}_{\mathrm{E},0}, \mathrm{D}_{\mathrm{E},0.5})$. The switching scheme of the estimation phase is similar as a $(L+2)$-bit fully differential SAR ADC. If V_{DAC} is positive, $\mathrm{C}_{\mathrm{n},L}$ will be switched to V_{ref}. Otherwise, $\mathrm{C}_{\mathrm{p},L}$ will be switched to V_{ref}. This operation will be repeated until the last conversion. Before the last comparison, $\mathrm{C}_{\mathrm{p},0}$ or $\mathrm{C}_{\mathrm{n},0}$ will be switched to V_{cm} according to the previous comparison result. Then the comparator completes the last comparison and gives the redundant output $\mathrm{D}_{\mathrm{E},0.5}$. After all conversion, the error voltage can be expressed as

$$V_{\mathrm{errp},L+M} = \frac{1}{2}\left(\mathrm{D}_{\mathrm{E},L}2^{L} + \cdots + \mathrm{D}_{\mathrm{E},0} + 0.5\mathrm{D}_{\mathrm{E},0.5}\right) \frac{V_{\mathrm{ref}}}{2^{L+M}} \tag{10}$$

The corresponding error code $\mathrm{D}_{\mathrm{errp},L+M}$ can be represented in decimal, as

$$\mathrm{D}_{\mathrm{errp},L+M} = \mathrm{D}_{\mathrm{E},L}2^{L-1} + \cdots + 0.5\mathrm{D}_{\mathrm{E},0} + 0.25\mathrm{D}_{\mathrm{E},0.5} \tag{11}$$

Figure 3 shows the output waveform of the DAC for estimating $V_{\mathrm{errp},11}$ in 12-bit SAR ADC during GEC phase with $M = 8$, $L = 3$ as an example.

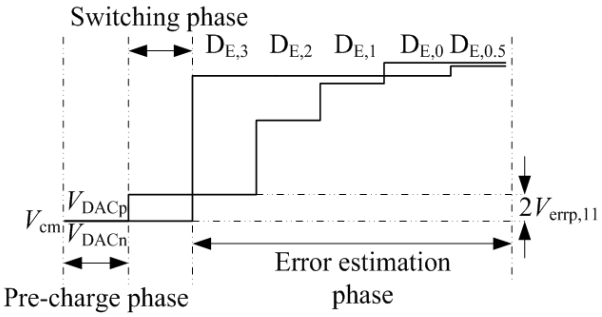


FIGURE 3. The output waveform of the DAC for estimating $V_{\mathrm{errp},11}$

The digital codes of the other error voltages due to the capacitor mismatches in the MSB-side part can also be achieved by this method.

After the GEC phase, SAR ADC goes into the normal conversion phase. The input voltages are sampled on the DAC and digitized into $(N+1)$-bit digital code of $(\mathrm{D}_{L+M}, \ldots, \mathrm{D}_{L}, \mathrm{D}_{L-1}, \ldots, \mathrm{D}_{0}, \mathrm{D}_{0.5})$. Then the raw digital code is summed with the error codes and the last two bits are discarded to get the corrected N-bit output code. Figure 4 shows the operation of the proposed digital-domain self-calibration technique. Thus, the corrected output code $\mathrm{D}_{\mathrm{out}}$ after calibration can be represented in decimal as

$$\mathrm{D}_{\mathrm{out}} = \left(2^{L+M} \times \mathrm{D}_{L+M} + \cdots + 0.5\mathrm{D}_{0.5}\right) + \left(\mathrm{D}_{\mathrm{err},L+M}\mathrm{D}_{L+M} + \cdots + \mathrm{D}_{\mathrm{err},L+1}\mathrm{D}_{L+1}\right) \tag{12}$$

where $\mathrm{D}_{\mathrm{err},i} = \mathrm{D}_{\mathrm{errp},i} + \mathrm{D}_{\mathrm{errn},i}$ $(i = L+1, \ldots, L+M)$.

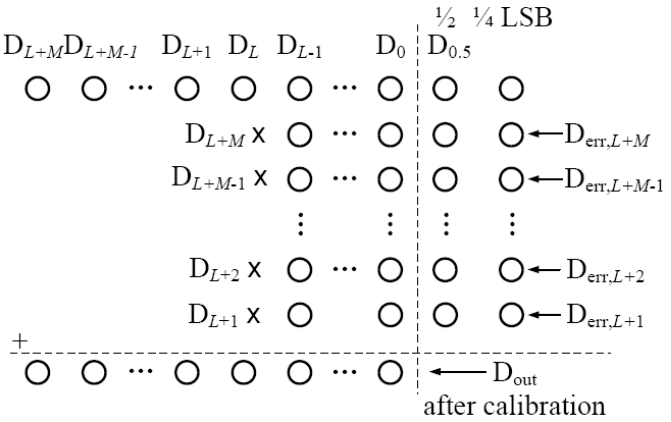


FIGURE 4. The operation of the proposed digital-domain self-calibration scheme

4. **Application Example and Simulation Results.** A 12-bit SAR ADC with the proposed digital-domain self-calibration technique is implemented in 40nm CMOS technology to demonstrate the effectiveness of the calibration technique. In addition, a low offset comparator is required to achieve accurate error values of capacitor mismatch. Thus, a dynamic comparator with offset calibration is applied [7]. For simplicity, the function of the adder in the proposed SAR ADC is implemented in PC. The layout of the proposed 12-bit SAR ADC is shown in Figure 5. The LSB-side part of DAC, which consists of 3-bit capacitor array and 1 redundant bit, is reused as a calibration DAC and the unit capacitor mismatch is 3%.

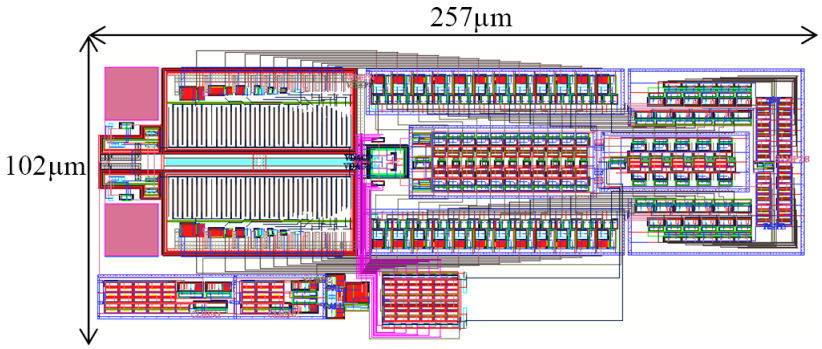


FIGURE 5. Layout of 12-bit SAR ADC with digital-domain self-calibration

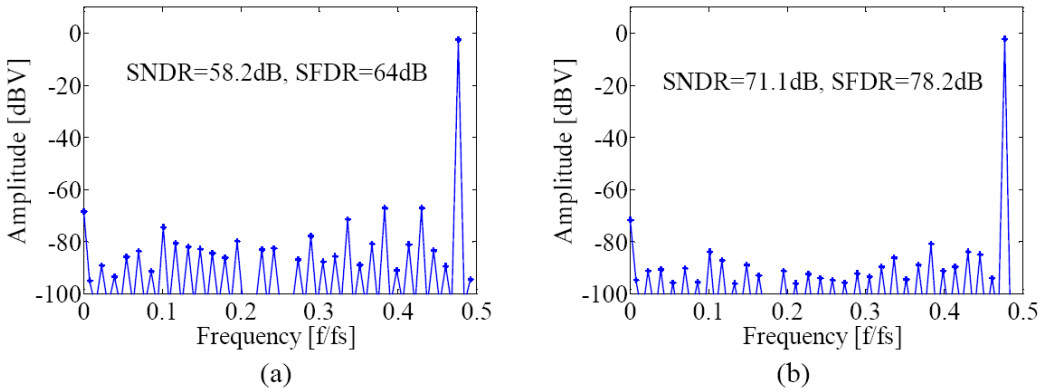


FIGURE 6. 12-bit SAR ADC output spectrum (a) before calibration; (b) after calibration

The plots of the 12-bit SAR ADC output frequency-spectrums before and after calibration are shown in Figure 6. After calibration, SNDR and SFDR are improved from 58.2 to 71.1dB and 64 to 78.2dB, respectively.

5. **Conclusions.** A digital-domain self-calibration technique is proposed to correct the error voltage due to the capacitor mismatch for SAR ADC. By using the proposed calibration technique, the capacitor match performance of fully differential binary-weighted SAR ADC is significantly improved without extra calibration DAC. Applied to a 12-bit SAR ADC with 3% capacitor mismatch, SNDR and SFDR are increased from 58.2 to 71.1dB and 64 to 78.2dB, respectively. In the future, the proposed digital-domain self-calibration technique can be expected to be applied to split-capacitor DAC to compensate for the nonlinearities.

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