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A CONTROL WAY OF A FIBONACCI SEQUENCE SWITCHED CAPACITOR DC-DC CONVERTER FOR HIGHER POWER EFFICIENCY

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Abstract. *In conventional power converters, magnetic components are necessary to design it. However, those components make the power converter heavy and bulky. For this reason, a switched capacitor (SC) DC-DC converter was proposed. The SC DC-DC converters are operated by controlling switches. The switches are controlled in the same duty ratio in conventional ways, although the converters have different instantaneous equivalent circuit in operating state of them. For this reason, the Fibonacci sequence SC DC-DC converter is targeted for this research in the sense that the converter has 3 different instantaneous equivalent circuit. We propose a novel control way of the converter to improve the power efficiency in this paper. The proposed control way is to control the duty ratio of the switches of the converter, while the conventional switching way is to fix the duty ratio. The characteristic of the proposed control way is clarified through theoretical analysis and SPICE simulation.*
Keywords: DC-DC converters, Switched-capacitor circuits, Fibonacci numbers, Step-up converters, Internal resistor

1. **Introduction.** A DC-DC converter is a kind of power converter to convert DC to DC. The common DC-DC converter consists of semiconductor switches, capacitors and magnetic components such as a transformer and an inductor. Those magnetic components make the size of the power converters heavy and bulky, and cause effects of the electromagnetic interference. For those reasons, a switched capacitor (SC) DC-DC converter was proposed as an alternative to DC-DC converters using magnetic components.

The first idea of SC converter was from an SC voltage multiplier proposed by Brugler [1]. Many types of SC DC-DC converters have been suggested with the first idea and the development of semiconductor switches. There are Fibonacci sequence type, switched capacitor voltage multipliers (SCVM) type, ring type and series-parallel type as the representative types of SC DC-DC converters [2-5].

Those converters are operated by changing a connection of the switches and the capacitors in them. Stretching the reach of this concept, there is an SC converter with 3 kinds of connection, which means that the SC converter is operated by 3 kinds of states. In previous researches, those SC converters are analyzed in the condition that all operation states for those SC converters have the same duty ratio of operation states respectively [2-6]. When an SC converter has the same instantaneous equivalent circuits at each operation state, the duty ratio has no influence on power efficiency of the SC converter in the steady state of it. However, when an SC converter has different instantaneous equivalent circuits at each operation state [6], it is necessary for higher power efficiency of it to control duty ratio of each operation state. The reason is that 'the different equivalent circuits' means 'the different internal resistors at each state'. Each internal resistor has influence on power efficiency of the SC converter. In this situation, controlling duty ratio

of each state is essential to operate an SC converter in higher power efficiency rather than fixing the duty ratio like the conventional ways in case of the SC converter with each different internal resistor at each operation state [1-6].

In this paper, it is shown how to set up the optimum duty ratio of an SC converter for better power efficiency. The Fibonacci sequence type SC converter is targeted because the target circuit has each different instantaneous equivalent circuit [6].

The organization of the rest of this paper is as follows. In Section 2, the circuit configuration of the Fibonacci sequence type SC DC-DC converter is shown. In Section 3, the theoretical analysis of the converter and the proposed switching way is implemented. In Section 4, the characteristic of the proposed switching way is verified by SPICE (simulation program with integrated circuit emphasis) simulation. Lastly, conclusion and future study are presented in Section 5.

2. **Circuit Configuration.** Figure 1 shows the circuit configuration of the target circuit which is denominated as the Fibonacci sequence switched capacitor DC-DC converter. In Figure 1, V_{in} and V_o are the input and output voltages of the target circuit, R_L is the load, S1∼S12 are switches and C1∼C5 are capacitors. The target circuit consists of 13 switches and 5 capacitors. The target circuit is operated by controlling those switches according to the switching way shown in Table 1. The reason that the title of the target circuit includes Fibonacci is that all capacitors are charged by the following Fibonacci sequence as shown in (1).

$$V_{Cn} = V_{Cn-1} + V_{Cn-2}, \tag{1}$$

where $n = \{3, 4, 5\}$ with $V_{C1} = V_{in}$ and $V_{C2} = V_{C1} + V_{in}$.

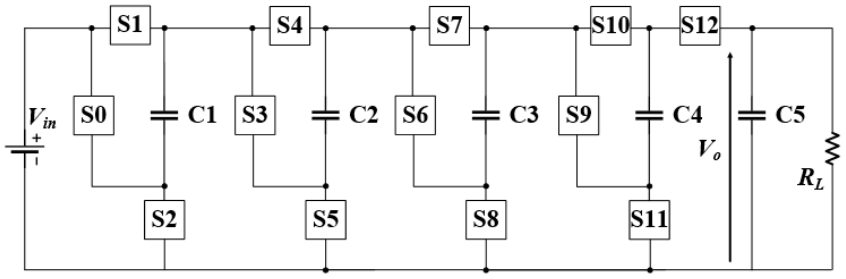


FIGURE 1. Target circuit

TABLE 1. Switching way

State	On	Off
T1	S1, S2, S3, S7, S8	Others
T2	S0, S4, S5, S6, S10, S11	Others
T3	S0, S3, S6, S9, S12	Others

In other words, odd number capacitors, C1 and C3, are charged by 1x and 3x stepped-up respectively in State-1. Even number capacitors, C2 and C4, are charged by 2x and 5x stepped-up respectively in State-2. In addition, C5 is not the capacitor for step-up but a smoothing capacitor. In State-3, all charged capacitors generate the 12x stepped-up and discharge the charged power to the lord.

3. **Theoretical Analysis.** In order to analyze the target circuit, theoretical analysis is implemented by using a four terminal equivalent circuit model as described Figure 2. The model consists of the ideal transformer and the SC resistance R_{SC}. R_{SC} can be obtained by using the on-resistance (R_{ON}) of all switches in this section. As you can see from

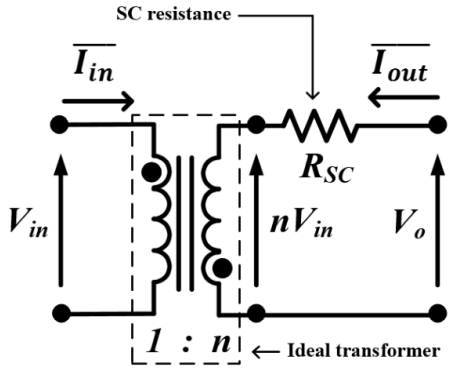


FIGURE 2. Four terminal equivalent circuit model

Figure 2, R_{SC} is the only one component in the model to consume the energy from the input power. Therefore, to derive the value R_{SC} of each state means that it is possible to compute theoretically power efficiency and output voltage. In this analysis, we make two assumptions as follows. 1) The switch in the target circuit is an ideal switch, except for having R_{ON}. 2) RC time constant is extremely larger than the system clock for all states.

In steady state, the amount of all capacitors' electric charge satisfies (2).

$$\sum_{i=1}^{3} \Delta q_{Ti}^{k} = 0, \text{ where } T = \sum_{i=1}^{3} D_i T = \sum_{i=1}^{3} T_i \text{ and } \sum_{i=1}^{3} D_i = 1. \tag{2}$$

In (2), Δq_{Ti}^{k} means the electric charge of the k-th capacitor in State-i. D_iT is the period of the system clock for State-i ($i = 1, 2, 3$). Each circuit equation as follows is given by using Kirchhoff's current law in each of the instantaneous equivalent circuits as shown in Figure 3.

$$\text{State-T1: } \Delta q_{T1,V_{in}} = \Delta q_{T1}^{1} - \Delta q_{T1}^{2},\ \Delta q_{T1,V_o} = \Delta q_{T1}^{5},\ \Delta q_{T1}^{2} = -\Delta q_{T1}^{3} \text{ and } \Delta q_{T1}^{4} = 0. \tag{3}$$

$$\text{State-T2: } \Delta q_{T2,V_{in}} = \Delta q_{T2}^{1},\ \Delta q_{T2,V_o} = \Delta q_{T2}^{5},\ \Delta q_{T2}^{3} = \Delta q_{T2}^{1} + \Delta q_{T2}^{2} \text{ and } \Delta q_{T2}^{3} = -\Delta q_{T2}^{4}. \tag{4}$$

$$\text{State-T3: } \Delta q_{T3,V_{in}} = -\Delta q_{T3}^{1},\ \Delta q_{T3,V_o} = \Delta q_{T3}^{4} + \Delta q_{T3}^{5} \text{ and } \Delta q_{T3}^{1} = \Delta q_{T3}^{2} = \Delta q_{T3}^{3} = \Delta q_{T3}^{4}. \tag{5}$$

Next, R_{SC} is obtained as (6) by using (3)$\sim$(5) and comparing the power efficiency's general form as (7). (7) is derived from the equivalent circuit model as shown in Figure 2. As you can see from (8), it can be confirmed that duty ratio, D_i ($i = 1, 2, 3$), has influence on power efficiency and output voltage.

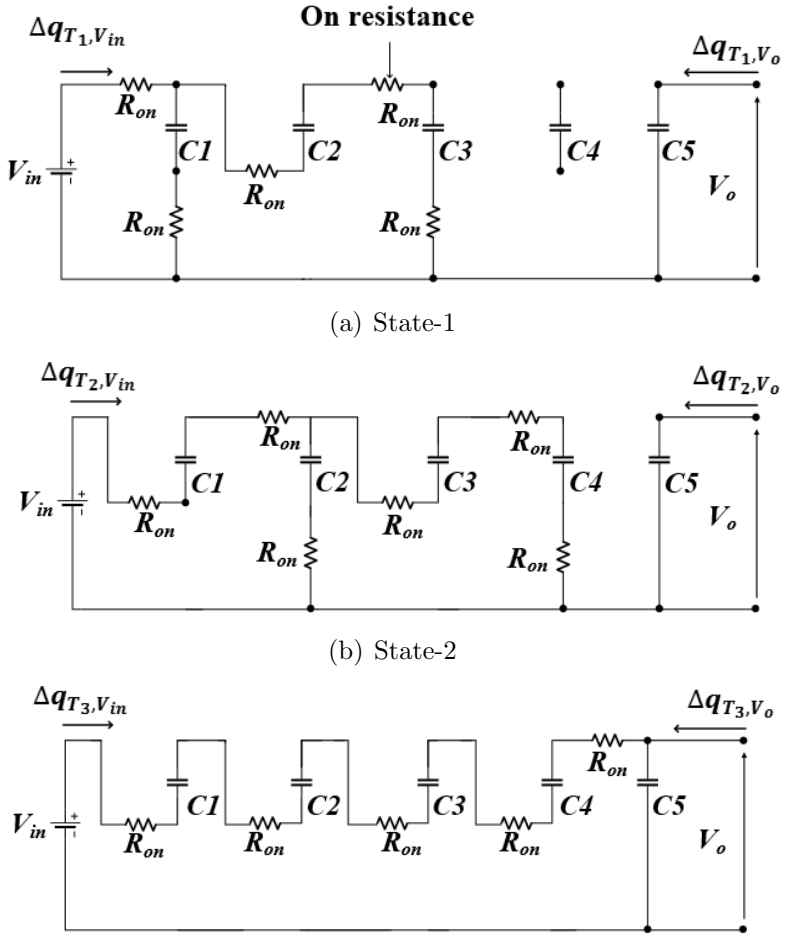
$$R_{SC} = \left(\frac{86}{D_1} + \frac{44}{D_2} + \frac{5}{D_3} \right) R_{ON} \tag{6}$$

$$W_T = \left(\frac{\Delta q_{V_o}}{T} \right)^2 \cdot R_{SC} \cdot T \tag{7}$$

$$\eta = \frac{R_L}{R_L + \left(\frac{86}{D_1} + \frac{44}{D_2} + \frac{5}{D_3} \right) R_{ON}} \text{ and } V_{out} = \frac{R_L}{R_L + \left(\frac{86}{D_1} + \frac{44}{D_2} + \frac{5}{D_3} \right) R_{ON}} \times 12V_{in}. \tag{8}$$

Table 2 describes the representative values of the efficiency and R_{SC} in each case of the duty ratio. Those values are derived by (8). To obtain those values, we fixed D1 from 1% to 98% and then changed D2 and D3 satisfying (2) respectively. Those values were calculated with the conditions as follows: 1) R_L is 100Ω and 2) R_{ON} is 0.85Ω.

In this theoretical analysis, we can know two facts as follows. 1) R_{SC} value is variable according to the duty ratio, which means there must be an optimal duty ratio for better power efficiency. 2) The target circuit with the switching way of controlling duty ratio



(a) State-1

(b) State-2

(c) State-3

FIGURE 3. Instantaneous equivalent circuit at each state

TABLE 2. Theoretical power efficiency

D1	D2	D3	Efficiency	R_{SC}
10%	67%	23%	11.046%	947.4
20%	60%	20%	18.212%	528.33
30%	52%	18%	22.769%	399.06
40%	45%	15%	25.368%	346.11
50%	37%	13%	26.318%	329.38
51%	37%	12%	26.327%	329.21
52%	36%	12%	26.324%	329.27
60%	30%	10%	25.707%	340
70%	22%	8%	23.389%	385.36
80%	15%	5%	19.022%	500.83
90%	7%	3%	11.666%	890.79
1/3	1/3	1/3	22.509%	405

has 3.818% higher power efficiency than the conventional way that is to fix the same duty ratio as 1/3.

4. **Simulation.** In this section, we present the simulation result of the target circuit and then compare the simulation result and theoretical result so that we prove whether the proposed switching way is suitable or not. The SPICE simulation was implemented under

TABLE 3. Simulation conditions

Parameter	Value
V_{in}	12 V
C1, C2, C3, C4	10 μF
C5	0.1 μF
R_{ON}	0.85 Ω
R_L	100 Ω
T	1.5 μsec

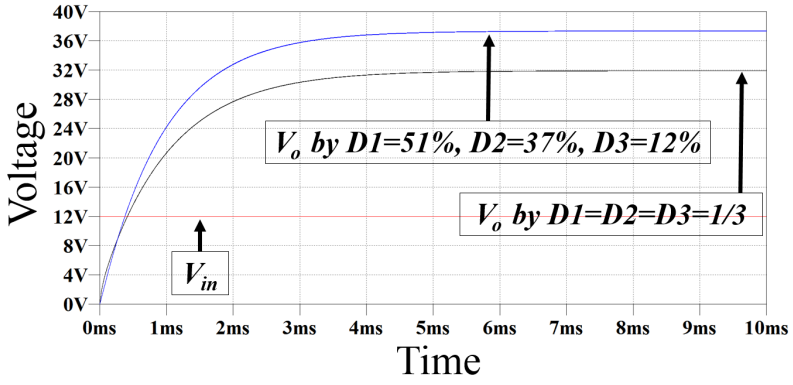


FIGURE 4. Simulated output voltage

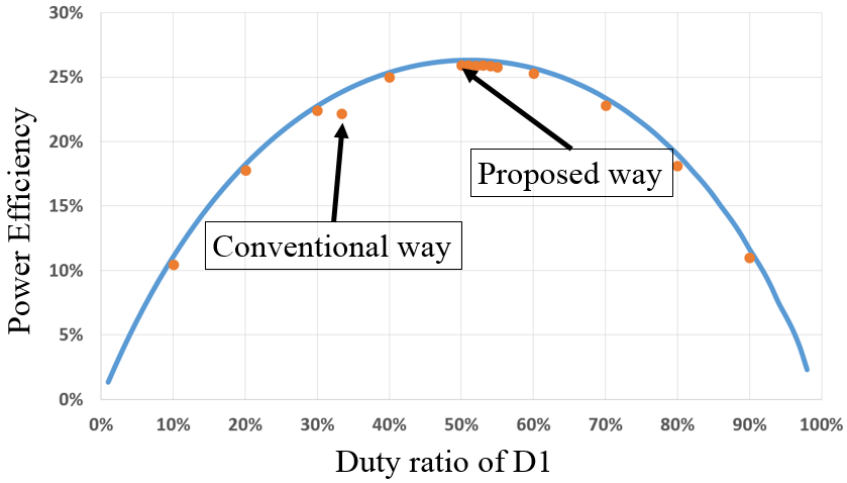


FIGURE 5. Simulated and theoretical power efficiency

the conditions as Table 3. Additionally, the duty ratios (D1, D2, D3) are set by using the way above-mentioned before section. Figure 4 shows the simulated output voltage of the target circuit in the highest power efficiency, duty ratio (D1 = 51%, D2 = 37%, D3 = 12%), and the conventional switching way (D1 = D2 = D3 = 1/3).

Figure 5 demonstrates the simulated power efficiency and theoretical calculation of power efficiency. As you can see from Figure 5, two waveforms follow a parabola graph, which means the value of waveform rises and then falls. Therefore, it is natural to have one of maximum values in the graph. The maximum power efficiency of the target circuit has 25.934% at the duty ratio: D1 = 51%, D2 = 37%, D3 = 12%. The simulated power efficiency with the proposed switching way can be higher than 3.774% by comparing with the conventional way having the same duty ratio as 1/3.

5. **Conclusions.** The control way of the Fibonacci sequence DC-DC SC converter has been proposed to improve the power efficiency of it in this paper. The proposed control way is to adjust the duty ratio of each state, while the conventional way is to fix the duty ratio as 1/3. The theoretical analysis was implemented to confirm which duty ratio is able to offer the highest power efficiency. The value of the duty ratio (D1 = 51%, D2 = 37%, D3 = 12%) was obtained, and we confirmed theoretically that the target circuit with the proposed switching way has 3.808% higher power efficiency than the conventional way. Next, we simulated the target circuit with the obtained duty ratio. The proposed switching way can achieve 3.774% higher power efficiency than the conventional way.

It is left as a future study to design the hardware of the target circuit with the proposed control way so as to prove practically the validity of it.

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