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AN FPGA-BASED SLIDING FUZZY CONTROL FOR DC/DC BOOST CONVERTER

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Abstract. *The Field Programmable Gate Array (FPGA) offers opportunities for improved performance and design flexibility for digital control. However, the complexity of Hardware Description Language (HDL) coding can be a barrier for the design engineer. Presented is a system modelling and development environment for FPGA-based digital control that also has the ability to auto-generate HDL code. The method uses HDL Coder tool technology in a MATLAB/SIMULINK environment to develop a digital fuzzy controller for DC/DC boost converter. The method presented provides complete boost converter simulation, while also providing the quality and productivity benefits of auto-code generation. Simulation and experimental results validated the validity of the control strategy presented in this paper.*
Keywords: Field Programmable Gate Array (FPGA), HDL Coder, Digital fuzzy controller, Boost converter

1. **Introduction.** As fossil fuel prices rise, as oil insecurity deepens, and as concerns about climate change cast a shadow over the future of coal, a new energy economy is emerging. The old energy economy, fueled by oil, coal, and natural gas is being replaced by one powered by wind and solar [1]. Therefore, the control technology of new energy power conversion is more required of fast response, accurate result and robust stablility.

Analog control has almost been replaced by digital one whose performance and quality of power converters [2] can be accepted. Most power electronics today are controlled by microprocessors. This is mainly due to the low-cost nature of these digital devices and high level of integration of peripherals such as analog to digital converters. Microprocessors are typically programed in C or assembly languages, which can be outside of the core expertise of most power engineers. However, when multiple parallel operations are to be executed by the same device, care must be taken to ensure proper performance. In contrast, an FPGA is an uncommitted "sea of gates". The device is programmed by connecting the gates together to form multipliers, registers, adders and so forth [3]. This can be done using Hardware Development Language (HDL), which places a dedicated resource for the task and allows for parallel operation. However, the complexity of HDL coding can be a barrier for the power engineer.

Tools of rapid prototyping FPGA control for variable speed drives have been developed and the use of FPGA technology has begun to penetrate power electronics control applications. The HDL coder of the MATLAB/SIMULINK tool provides graphical design blocks and the ability to auto-generate HDL code in the MATLAB/SIMULINK environment. The HDL coder has an expansive library of common control functions to speed up the development of control applications and can provide a holistic system model which gives valuable understanding of the design prior to building hardware. This paper presents a

method of developing an FPGA-based control by the HDL coder to handle the controlled analog plant of the DC booster circuit.

Because the dynamics of the DC converter with control are high order, where dominant poles have a time constant below 0.3ms, the general microcontroller is a serial implementation of program, and it is difficult to achieve "against the instant impedance changes to increase the relatively stable output voltage". In order to speed up the processing of data, recently the FPGA chip with parallel computing was used to linearly control the DC/DC converters [4,5] based on small signal analysis. Traditional linear control is week robustness in load varying and output noise for linear controlled model. In this paper, we do not analyze the linear model of the system because many uncertain parameters can disturb the establishment of the linear model. On the contrary, we directly construct a nonlinear sliding fuzzy control based on the FPGA hardware chip to handle the DC/DC converter with uncertainty to enhance the robustness of the closed loop system.

Recently switching power supplies are widely applied in various fields for their light weight, compact size, high efficiency and reliability. DC power converters are the main components of switching power supplies. There is much literature [6-10] focusing on the control strategies to improve dynamic behavior of DC-DC power converters. The control of DC/DC converter is one of the hot topics. Fuzzy control has been reported to be successfully used for a number of complex and nonlinear process, including DC/DC power converters, robotics [11], and renewable energy systems [12]. Fuzzy control is often constructed based on expert knowledge which requires extensive trial and error tuning. Thus, a more systematic approach with less expert knowledge for fuzzy control is desired. Variable structure control with sliding mode was first introduced in the 1950s [13,14]. It is a powerful, systematic design method that can yield a closed loop system that is very robust against plant uncertainties and external disturbances. In theory, the sliding mode controlled system can be entirely independent of effects due to modeling uncertainties, parameter fluctuations and disturbances. DC/DC converters are inherently variable structured because of the switching action. Therefore, variable structure control with sliding mode is a suitable control solution for DC-DC converters [15]. This paper presents the fuzzy controller based on the principles of variable structure to regulate the output voltage of a boost converter. The proposed one combines the advantage of both fuzzy control and variable structure control. The variable structure approach facilitates the fuzzy controller's design and implementation. This paper is organized as follows. The configuration of a fuzzy control system for the boost converter is viewable in Section 2. Section 3 proposes the design and tuning of a fuzzy control using variable structure. An illustrative example to show the simulation result is given in Section 4. Conclusions are summarized in Section 5.

2. **Problem Statement.** A DC boost converter can be regarded as a second order system with nonlinear property. The Fuzzy Pulse Width Modulation (PWM) controller is proposed to control the DC boost converter's output voltage V_o approaching the desired one V_r in Figure 1. The boost convert can be expressed generally in two sets of state equation which depends on the position of power switch element Q in Figure 1.

If the switch Q is in position on, the inductor voltage can be obtained, from KVL, as

$$\frac{di_L}{dt} = \frac{V_{in}}{L} \tag{1a}$$

$$\frac{dV_o}{dt} = -\frac{V_o}{RC}. \tag{1b}$$

The other one is obtained if the switch is in off position.

$$\frac{di_L}{dt} = \frac{V_{in} - V_o}{L} \tag{2a}$$

$$\frac{dV_o}{dt} = \frac{i_L}{C} - \frac{V_o}{RC}. \tag{2b}$$

Two distinct Equations (1) and (2) are weighted by the duty ratio and superimposed as $(d) * (1) + (1 - d) * (2)$:

$$\frac{di_L}{dt} = \frac{V_{in} - (1-d)V_o}{L} \tag{3a}$$

$$\frac{dV_o}{dt} = \frac{(1-d)i_L}{C} - \frac{V_o}{RC} \tag{3b}$$

where $d \in [0\ 1]$ is the duty cycle regarded as control input. Next we set the inputs of FLC are the error e between V_r and V_o, and the Δe, difference of error e, respectively, which are defined as

$$e(k) = V_r - V_o \tag{4}$$

$$\Delta e(k) = e(k) - e(k-1) \tag{5}$$

where V_o is the actual output voltage of DC/DC converter at the kth sampling, and V_r is the desired reference voltage. The output of the FLC is defined as a duty ration difference of $d(k) - d(k-1)$, at the kth sampling time, written as

$$d(k) = d(k-1) + \delta(k) \tag{6}$$

$$\delta(k) = FLC(e(k), \Delta e(k)) \tag{7}$$

where $\delta(k)$ is the consequent part of the proposed Fuzzy Logic Controller (FLC) and is added to the previous sampling period's duty cycle $d(k-1)$. Then input $d(k)$ in (6) is sent to DC/DC converter's switch Q to generate output voltage following reference one. From (6) we know that the signal $\delta(k)$ of the FLC output can affect the PWM duty cycle $d(k)$ to improve steady-state error. That is, the main task of this paper is to design $\delta(k)$ in (7)

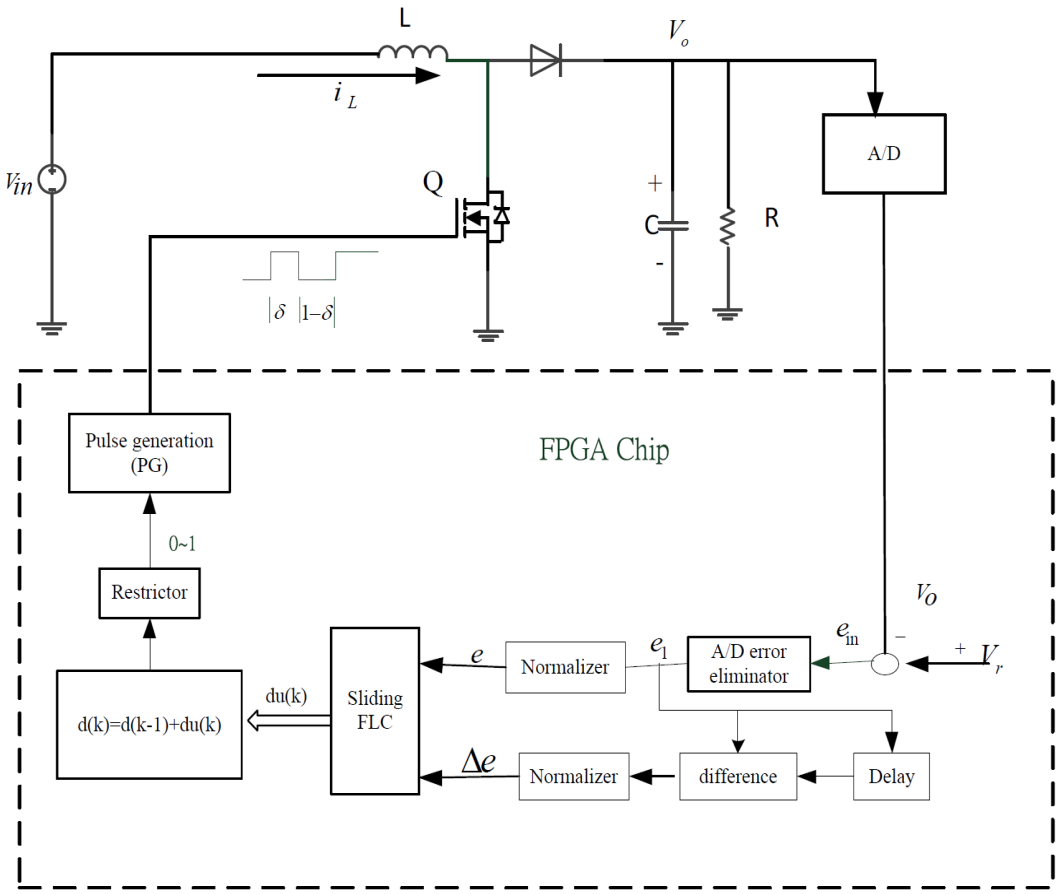

FIGURE 1. DC/DC boost converter with FPGA control chip

to handle the output voltage V_o approaching the desired reference V_r under variation of load R or input voltage source V_{in}. No complicated arithmetic expression is needed, but a linguistic control variable to do is a character of fuzzy logic system. The configuration is shown schematically in Figure 1.

3. **Fuzzy PWM Controller Based on Sliding Mode.** The block diagram of the FLC controller based on sliding mode for DC/DC converter is shown in Figure 1. This proposed controller is composed of Pulse Generation (PG) and Sliding Fuzzy Logical Control (FLC) whose rule table is constructed by sliding mode. The FLC can be divided into four modules: (i) fuzzification is the classification of input data into suitable linguistic values or sets; (ii) knowledge base includes rule base and data base; (iii) decision making is inferring control action from rule base; (iv) defuzzification is the conversion of the inferred fuzzy value of real crisp value.

Before designing the FLC, we describe why to construct A/D error elimination and what it means. Take an example to explain. Analog signal 2.3 volt inputs into A/D (analog converter digital) conversion whose specification is 10-bit data bus and operational voltage 5 volt. The principle of A/D conversion is to cut 5 volt into $2^{10} - 1 = 1023$ equal parts and to analyze that the input voltage 2.3 is located 471st in 1023 equal parts. Then 471 multiplied by the size of each section 5/1023 becomes 2.30252278. This $2.30252278 - 2.3 = 0.002052278$ error is what we mean "A/D (analog-to-digital converter) error", inherent error of A/D converter. If not eliminating this A/D error, the signal entering the FPGA chip is not really the original one. This will affect the digital control capability. In order to correct this inherent error of A/D converter, this paper proposes an eliminator whose mathematical representation is shown as below:

$$e_1 = \frac{e_{in} - err}{1 - err}, \text{ for } e_{in} > 0 \tag{8}$$

$$e_1 = \frac{e_{in} - err}{1 + err}, \text{ for } e_{in} \leq 0 \tag{9}$$

where $e_{in} = V_r - V_o$, err is the preset error value, and above mentioned example $err = 0.002052$.

Before entering the FLC, input signals must first be normalized as follows:

$$\underline{e} = \frac{e_1}{|\underline{e_1}|}; \text{ for } \underline{e_1} < e_1 < 0 \tag{10a}$$

$$\overline{e} = \frac{e_1}{|\overline{e_1}|}; \text{ for } 0 \leq e_1 < \overline{e_1} \tag{10b}$$

where e_1 is the input signal of normalization which ranges between lower bound $\underline{e_1}$ and upper one $\overline{e_1}$. The output of normalization is e whose range is between -1 and 1 in Figure 1. This operator performs normalization between e and e_1, named as

$$e = normalize(e_1) \tag{11}$$

where e_1 is described in (8) and (9).

Rewrite (6) and (7)

$$d(k) = d(k-1) + \delta(k)$$

$$\delta(k) = FLC\left(e(k), \Delta e(k)\right).$$

We take the e and Δe as the antecedent part of the proposed FLC to produce the change $\delta(k)$ in a duty ratio between 0 and 1 and then pass it to accumulator (6). The FLC is shown to be of Takagi-Sugeno type and uses a control strategy expressed linguistically by the form:

$$Rule^{(i)}: \text{ if } e \text{ is } X_1^{(i)} \text{ and } \Delta e \text{ is } X_2^{(i)} \text{ then } \delta = Y^{(i)} \tag{12}$$

where $Rule^{(i)}$ is the ith control rule, $X_j^{(i)}$ and $Y^{(i)}$ denote the fuzzy sets of the ith rule defined on e, Δe and δ, respectively. The Mean of Maximum (MOM) is referred as defuzzification strategies shown as

$$y^* = \frac{1}{N}\sum_{j=1}^{N} y_j \tag{13}$$

where y_j is the jth highest degrees in that corresponding membership function. FLC's membership function is a triangular shape of this paper. The shape of the membership functions associated with the input fuzzy levels does not affect the stability issue. Design rule base is based on the concept of sliding mode. Set a digital slide plane

$$S\left(e(k), \Delta e(k)\right) = \frac{\Delta e(k) = e(k) - e(k-1)}{T} + \lambda e(k) \tag{14}$$

where T is the sampling time of A/D conversion. This fuzzy rule base can be derived based on this principle of variable structure control in Table 1 in which the input variables in the antecedent part of the rules are e, Δe and the consequent part is δ of the output variable. The linguistic representation of fuzzy sets P, BP, MP, Z, MN, BN, and N are "positive", "best positive" "medium positive", "zero", "medium negative", "best negative", and "negative". The antecedent sets and consequent one are chosen as (P, Z, N) and (BP, MP, Z, MN, BN), respectively. The rules in Table 1 are read as, taking rule 1 as an example, "Rule 1: if e is P and Δe is P, then δ is BN". The degree of membership functions $\mu_i(e, \Delta e) \in [-1, 1]$ and $\mu_i(\delta) \in [0, 1]$ is obtained for each rule. Traditionally, it is necessary to construct the rule table of fuzzy system by in-depth knowledge of the plant. And it will waste time to try and error to tune fuzzy rule and membership function. Here we use a variable structure approach to overcome this drawback for obtaining satisfactory system performance of DC-DC converter.

Table 1. 3×3 rule base of FLC

e \ Δe	N	Z	P
P	Z	MN	BN
Z	MP	Z	MN
N	BP	MP	Z

In short, the procedure constructing the sliding FLC based on FPGA chip is summarized as follows:

(i) Simulate Figure 1 in MATLAB/SIMULINK platform;
(ii) If simulation performance of Step (i) is ok, then rewrite the program of Step (i) by using the HDL Coder tool of MATLAB/SIMULINK;
(iii) Check the performance of Steps (i) and (ii) is equiavlent (go to next step) or not (go to Step (ii));
(iv) Rebuild the Verilog code from Step (ii) in the Quartus II platform;
(v) Check the performance of Step (iv) satisfies desired performance (go to next step) or not (go to Step (ii)).
(vi) Download executing file into an ALTERA FPGA chip.

4. **Experimental Results.** The parameters of boost converter Figure 1 are L = 50H, C = 1000F, R = 25, PWM frequency f = 150Khz. Based on the rule in Table 1, the boost converter topology with the FLC was modeled in Figure 2 using MATLAB/SIMULINK. The SimPower System toolbox is required to model the power electronics section.

In order to test the proposed FLC's robustness against input voltage and load resistance variation, we set the input voltage varied from 4 to 7 and load resistance varied from 12.5Ω

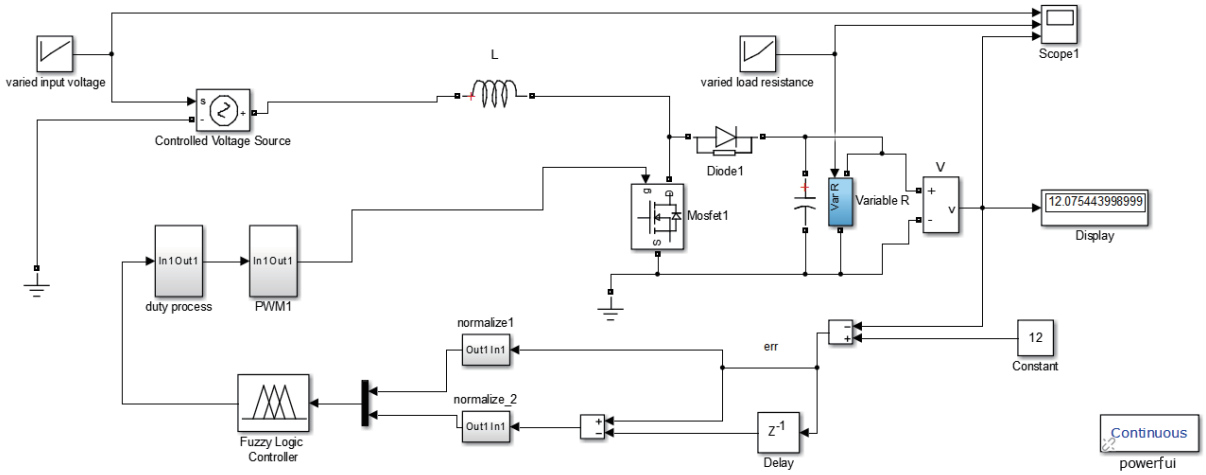

FIGURE 2. MATLAB/SIMULINK model for DC/DC converter with sliding FLC control

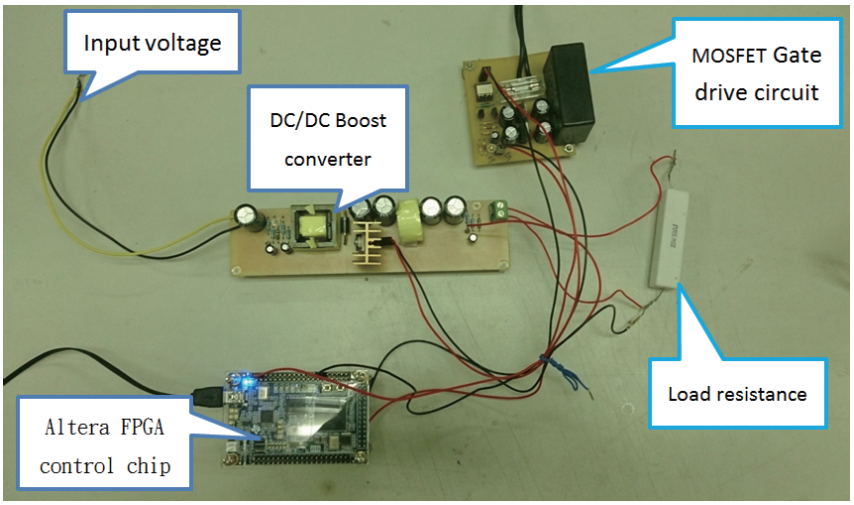

FIGURE 3. DC Converter with FLC based on Altera FPGA development board

to 50Ω. The circuit implementation of Figure 1 is shown in Figure 3 with FPGA chip number Altera Cyclone IV EP4CE2F17C6N. The HDL code inside FPGA chip of Figure 1 can be directly constructed by using the proposed design process. A varied input voltage $4 \sim 7$V, varied resistance load $12.5\Omega \sim 50\Omega$ and reference voltage 12V are set in hardware circuit in Figure 3 whose performance is shown in Figure 4. Viewing from Figure 4, the proposed digital control design indeed meets the robustness against input/load variation.

5. **Conclusions.** A complete new robust FLC controller based on FPGA implementation for DC/DC boost converter has been proposed. With input voltage and load resistance variation, the proposed FLC still can handle the output voltage to attain desired one. Traditional fuzzy controller with more rules needs more time to defuzzify computation, however, this study used the simplest fuzzy rules to minimize the fuzzy engine calculation time and experimental results also show the proposed method's effectiveness.

Parallel computing and high-speed data processing of FPGA chip can be applied to wireless transmission, voice or image processing in future research. However, the different communication interface for FPGA chip must first be solved such that its application can be widely developed. The future use of FPGA chip will be comprehensive in different areas.

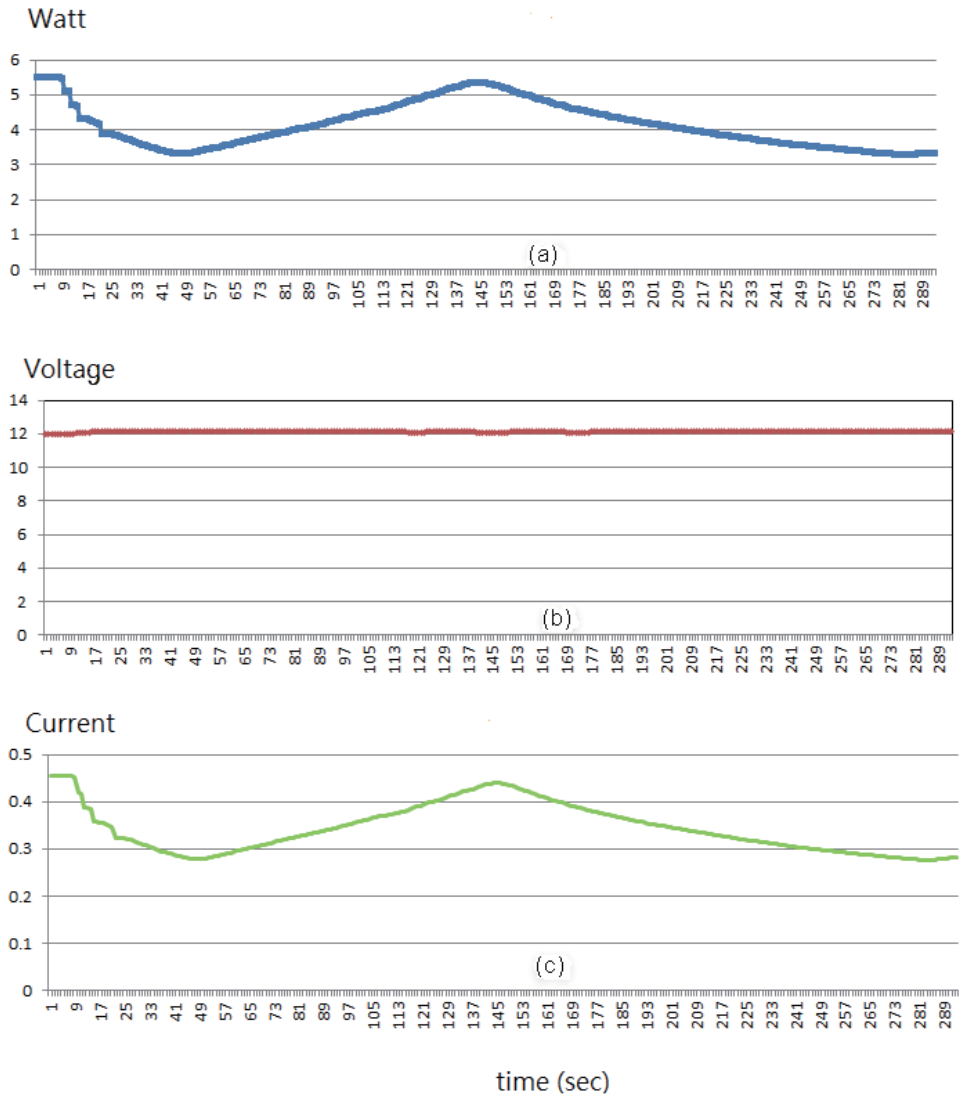

FIGURE 4. System performance under input voltage 4 $\sim$ 7 volts, varied load 12.5Ω $\sim$ 50Ω and the reference voltage 12 volts: (a) load power; (b) load output voltage; (c) load current

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REFERENCES

[1] T. S. Francisco, C. Peralta, L. G. Oscar, J. Navarro and I. Cruz, Effect of roof-mounted solar panels on the wind energy exploitation on high-rise buildings, *Journal of Wind Engineering and Industrial Aerodynamics*, vol.145, pp.123-138, 2015.

[2] D. Guilbert, A. Gaillard, A. Mohammadi, A. N'Diaye and A. Djerdir, Investigation of the interactions between proton exchange membrane fuel cell and interleaved DC/DC boost converter in case of power switch faults, *International Journal of Hydrogen Energy*, vol.40, pp.519-537, 2015.

[3] E. Monmasson and M. Cirstea, FPGA design methodology for industrial control systems – A review, *IEEE Trans. Industrial Electronics*, vol.54, pp.1824-1842, 2007.

[4] U. Sadek, A. Sarjaš, R. Svečko and A. Chowdhury, FPGA-based control of a DC-DC boost converter, *IFAC-Papers*, vol.48, pp.22-27, 2015.

[5] J. S. Prasad, Y. P. Obulesh and C. S. Babu, FPGA (field programmable gate array) controlled solar based zero voltage and zero current switching DC-DC converter for battery storage, *Energy*, vol.106, pp.728-742, 2016.

[6] Y. M. Park, U. C. Moon and K. Y. Lee, A self-organizing a fuzzy logic controller for dynamic systems using a fuzzy auto-regressive average model, *IEEE Trans. Fuzzy Systems*, vol.3, pp.75-82, 1995.

[7] L. X. Wang, Stable adaptive fuzzy logic controller of nonlinear systems, *IEEE Trans. Fuzzy Systems*, vol.1, pp.146-155, 1993.
[8] C. Elmas, O. Deperlioglu and H. H. Sayan, Adaptive fuzzy logic controller for DC-DC converters, *Expert Systems with Applications*, vol.36, pp.1540-1548, 2009.
[9] C. P. Ugale, R. B. Dhumale and V. V. Dixit, DC-DC converter using fuzzy logic controller, *International Research Journal of Engineering and Technology*, vol.2, pp.593-596, 2015.
[10] N. F. N. Ismail, I. Musirin, R. Baharom and D. Johari, Fuzzy logic controller on DC/DC boost converter, *2010 IEEE International Conference on Power and Energy*, Kuala Lumpur, Malaysia, pp.661-666, 2010.
[11] I. R. Fdez, M. Mucientes and A. Bugarín, Learning fuzzy controllers in mobile robotics with embedded preprocessing, *Applied Soft Computing*, vol.26, pp.123-142, 2015.
[12] X. X. Yin, Y. G. Lin, W. Li, Y. J. Gu, P. F. Lei and H. W. Liu, Sliding mode voltage control strategy for capturing maximum wind energy based on fuzzy logic control, *International Journal of Electrical Power & Energy Systems*, vol.70, pp.45-51, 2015.
[13] V. Utkin, J. Guldner and J. X. Shi, *Sliding Mode Control in Electromechanical Systems*, Taylor and Francis, 1999.
[14] V. Utkin, *Sliding Modes in Control Optimization*, Springer-Verlag, 1992.
[15] L. Guo, J. Y. Hung and R. M. Nelms, Comparative evaluation of sliding mode fuzzy, controller and PID controller for a boost converter, *Electric Power System Research*, vol.81, pp.99-106, 2011.