

STRUCTURE SYNTHESIS FOR PASSIVE FAULT-TOLERANT DIGITAL LOW PASS FILTERS WITH PERMANENT FAULTS

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ABSTRACT. *Fault tolerant digital filters are widely expected for use in modern electronic systems. In this letter, a structure evolution based optimization algorithm (SEOA) for designing an infinite impulse response (IIR) digital low pass filter is proposed. The filter structure is synthesized in SEOA for passive fault tolerance against permanent circuit element failures, such as short and open circuits. In SEOA, a filter structure is generated from a node and grows up by attaching multipliers and delay elements to it one by one. The structure is encoded and then is evolved based on genetic algorithm (GA). GA's operations are redesigned to ensure structures are evolved validly and efficiently. Simulation results show filter performance is greatly affected by multiplier failures. Compared with the classic IIR digital filter implementations, SEOA improves fault tolerance of digital low pass filters when they suffer permanent mixed circuit faults of multipliers.*

Keywords: Digital filters, Fault tolerance, Evolutionary algorithms, Filter structures

1. Introduction. Digital filters have been widely used [1, 2] in electronic devices. In some areas, it is expected the digital filter has a strong fault tolerance. For example, the outer space circuits are expected to tolerate a certain degree of cosmic particle impact; critical computing, such as nuclear computing, is expected to tolerate occasional failures without affecting final results. Some faults, such as soft errors, transiently change the states of a digital element, which produces temporary effects on the digital system. Some fault tolerant techniques have been proposed for such kind of faults.

The relative techniques can be classified into two categories. The first category designs redundant modules to correct soft errors. The traditional approach, known as triple modular redundancy (TMR), has been to triplicate the elements that can suffer soft errors and add the voting logic to select the majority in case of an error. When soft errors can affect both combinational and sequential logic elements, the usual approach is to triplicate the entire block, which results in a large area and power consumption. Single-event upset (SEU) is often used as a fault type of soft errors. A novel residue number (RN)-based method was proposed in [3] against SEU. The proposed method applies the transpose form of the finite impulse response (FIR) filter to avoiding the fault missing caused by SEU on shift registers. It also adjusts the input intelligently to avoid the fault missing on the filter coefficients. After all the fault missing events are avoided, the modulus can be minimised to achieve the minimum overhead. A redundancy-based fault-tolerant methodology is proposed in [4] to design highly reliable analogue and mixed-signal circuits. The key contribution of the proposed work is improving the reliability of analogue and mixed-signal circuits using an innovative mean voter. The mean voter is a low-power, small area, very high bandwidth and linearly scalable unit; and it works for both odd and even redundancy factors.

The second category designs algorithms to recover soft errors. Energy-efficient soft error-tolerant techniques for digital signal processing (DSP) systems were presented in [5]. The proposed technique, referred to as algorithmic soft error-tolerance (ASET), employs low-complexity estimators of a main DSP block to achieve reliable operation in the presence of soft errors. Three distinct ASET techniques: spatial, temporal and spatio-temporal are presented. For frequency selective FIR filtering, it provides robustness in a SEU scenario. The power dissipation of the proposed techniques is lower than TMR. Based on the ASET technique, reasonable reliability with reduced cost and power consumption is provided for adaptive filters [6]. In [7], the idea of applying coding techniques to protecting parallel filters is addressed in a more general way. It enables a more efficient protection that filter inputs and outputs are represented by numbers instead of bits. This reduces the protection overhead and makes the number of redundant filters independent of the number of parallel filters. In [8], parallel filters are protected using error correction codes (ECCs) in which each filter is the equivalent of a bit in a traditional ECC. This new scheme allows more efficient protection when the number of parallel filters is large. The correlation between the different filters is used for fault detection and recovery in [9], so that the redundant filters that are needed in existing solutions can be removed, which reduces the implementation cost. [10] aims to improve fault tolerance of a class of open quantum systems coupled to a laser field that is subject to stochastic faults. A quantum-classical bayesian inference method was proposed based on the analysis of this class of open quantum systems, which is used as a kernel to design a fault tolerant quantum filter. A novel approach is proposed in [11] for designing fault-tolerant filters whose measurements undergo quantization. The proposed filter consists of two robust filters which operate in two different zones. These zones are defined based on the effects of the quantization on the residual signal between the quantized measurement and the one generated by the filter.

All of above reports are all concerned on soft errors. As the best of our knowledge, the research on permanent faults for digital filters have still not been reported. In real life situation, however, certain outer reasons, such as environmental humidity, particle and electromagnetic interference, may cause damage to the filter circuit elements. In long-term unattended environments, some of digital filter components may be destroyed permanently.

In this letter, the fault tolerance of the digital filter is investigated against permanent circuit faults of multipliers. A structure evolution based optimization algorithm (SEOA) is proposed to design the infinite impulse response (IIR) digital filter. This approach improves genetic algorithm (GA) [12, 13] to optimize the filter structure and strengthens fault tolerance of the filter. No evolutionary algorithms have been proposed for structure synthesis of digital filter with passive fault tolerance. By comparing SEOA with some classic implementations of digital filters, the simulation shows the digital filter designed in this letter has excellent fault tolerance.

The organization of the paper is as follows. In Section 2, the proposed algorithm, SEOA, is elaborated at length, which aims to design fault tolerant IIR low pass digital filters with permanent faults. The experimental results are provided under different fault rates in Section 3. Finally, we give a conclusion in Section 4.

2. Algorithm Design. The proposed algorithm SEOA designs digital filter structures based on GA. GA has the potential of holding high performance for those problems with varied-length chromosomes [13]. In SEOA, filter structures with different sizes are coded as chromosomes with different lengths. As depicted in Figure 1, filter structures are generated to form initial population of the chromosomes. These structures are crossed with each other at a crossover probability, and then mutated at a mutation probability. The best population-size filter structures are handed down to next generation of evolution.

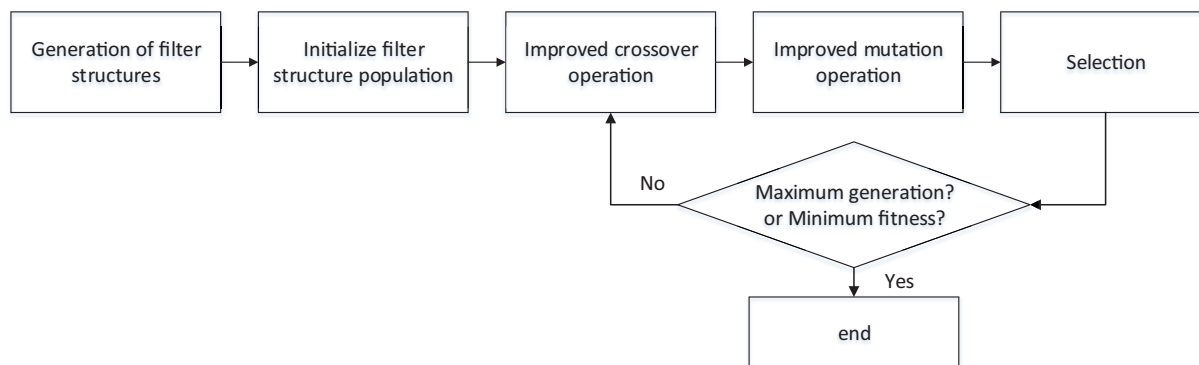


FIGURE 1. The flowchart for designing a digital filter in SEOA

With chromosome evolution, the fitness of structures decreases until GA reaches a maximum generation or the fitness satisfies given conditions. Three issues are associated with addressing the problem. The first is to encode a digital filter structure. The second is to cross two structures. Crossover in GA is difficult to be applied to circuit individuals, because correct circuits may become illegal when they cross with each other. The third is to evaluate a structure. The following represents our algorithm to solve these three issues.

2.1. Generation of filter structures. At first, a filter structure is elaborately created with digital components. The creation method not only works with crossover operators, but also carries with an ability of fault tolerance. A digital linear structure is generated by attaching delay elements and multipliers to it one by one. An active node is defined as a node to which a new attached element must be linked with its one terminal. The other terminal of the new element has two choices. The first one is linking itself to a newly created node. The new node becomes an active node, and the old active node becomes a nonactive node. A structure has only one active node at the same time. The second choice is to link itself to a nonactive node. The two choices are random with equal probability. The attachment of a new element can be formatted as an instruction of $|V_i|V_o|P_c|T_{com}|$, where V_i and V_o are the linked nodes in a filter structure. Signals of the element flow from V_i to V_o . T_{com} indicates the element type. P_c is the element's parameter. All instructions of an established structure create an instruction sequence, which has encoded a digital structure and is seen as a chromosome of GA. The creation of a filter structure, where one or more than one components are put between any two nodes, implies that any two nodes have a comparable probability to provide a backup branch. As we know, parallel branches are an effective way to increase fault tolerance of a system. Backup branches within a structure will validly protect the local signal flow between nodes. Damage of a component within a structure does not totally destroy a system. With such a component level backup, a filter structure is substantially strengthened against faults.

2.2. Evolution of filter structures. Filter structures are optimized through evolution based on GA. GA operators, i.e., crossover, mutation and selection operate the filter structure seen as the chromosome generation by generation. Crossover between two chromosomes essentially is to cross two structures. Crossover strategies, however, in this case often get into a dilemma, because two structures are difficult to maintain their validity when they are crossed. The design of the filter structure takes the problem into account, which is effective to cooperate with a single point crossover between two structures.

A crossover strategy is designed based on the filter structure. A crossing point divides an instruction sequence into two parts. The crossover causes an exchange of the front parts or the rear parts of the two sequences. Considering the generation of a digital

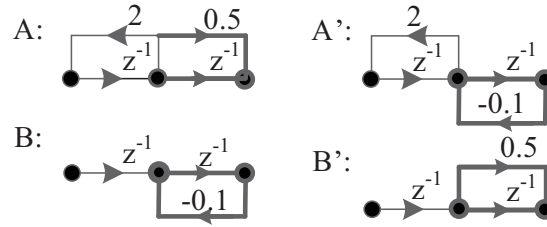


FIGURE 2. An example of the crossover operation

structure, the two new sequences are valid when the two crossing points have the same number of N_i . Under the condition, the front part of one structure grows according to the way of the rear part of the other structure. An example is shown in Figure 2. The crossing point is at the second node of their structures, as described two parts of thick lines and thin lines in Figure 2. A' and B' are the crossed structures from A and B. They are valid when A and B are valid.

In the mutation stage, we make a considerable mutation on chromosomes. Every selected chromosome is replaced by a newly created chromosome, which has the same length with its predecessor. This allows the chromosome transition from a point to another totally different point in the solution space. In the selection stage, we sort the chromosomes by their fitness. P_s chromosomes with the smallest fitness will be kept down as the next generation of chromosomes, where P_s is the population size.

The fitness is designed with respect to the frequency response error. The transfer function of a digital filter is derived from its structure as described in [14]. An internal signal in the system is expressed as output of a node.

$$\mathbf{W}(z) = (\mathbf{I} - \mathbf{Q}(z))^{-1}\mathbf{P}(z). \quad (1)$$

\mathbf{W} records expressions of internal signals. \mathbf{I} is an identity matrix. \mathbf{Q} is a connection matrix, which indicates the relations among internal signals. \mathbf{P} denotes a vector which records gains or delay from the system input signal to internal signals. The transfer function of the structure is

$$H(z) = \mathbf{W}_{out}(z), \quad (2)$$

where *out* is the identified number of the system output node.

In SEOA, $H(z)$ is discretized by substituting $e^{j\pi i/n}$ for z . $H(K_i)$ gets the i th value of n samples of the frequency response.

$$H(K_i) = H(z)|_{z=e^{j\pi i/n}}. \quad (3)$$

A chromosome is evaluated through calculating its frequency response error. Fitness, defined as the error, is estimated in

$$fitness = \frac{1}{n} \sum_{i=1}^n \log^2 \left(\frac{|H(K_i)|}{|D(K_i)|} \right), \quad (4)$$

where $D(K)$ is the desired frequency response in a discrete form. The n is the number of sampling points.

3. Main Results. The design specifications of magnitude frequency responses of IIR digital low pass filters are set. Passband ranges from 0 rad to 0.45π rad, stopband from 0.6π rad to π rad, the minimum of passband attenuation is 3 dB and the maximum of stopband attenuation is 60 dB. Simulation parameters are given in Table 1. The multipliers suffer concurrent faults in short and open circuits with the same fault rate ranging from 0.01 to 0.05. That means 1%-5% multipliers in a structure are in fault. They fall into either a short circuit or an open circuit. The faults are concurrent and permanent. The test reveals fault tolerance of the filter structure.

TABLE 1. The parameter settings of the proposed algorithm

Parameter	Value	Parameter	Value
Crossover rate	0.7	Mutation rate	0.1
Population size	100	Chromosome length	50
Maximum generation	10000	Multiplier gain	$[-2, 2]$
Sample rate	128		

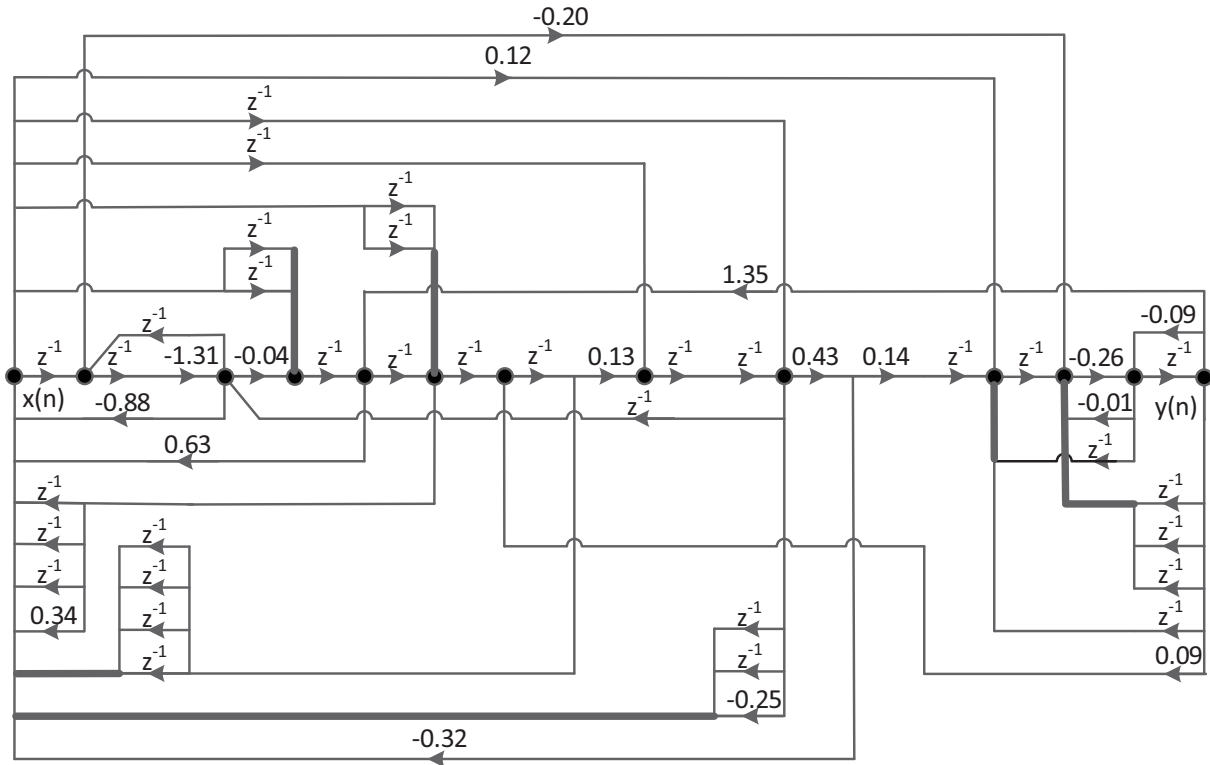


FIGURE 3. The structure of the digital filter designed by SEOA

The structure designed in this letter is shown in Figure 3. In the structure, multiplier gain is given 2 decimal places. The solid circle is denoted as adders, arrows with a note z^{-1} are delay elements and other arrows with a floating point number are multipliers. A thin line in the structure indicates a single wire and a thick line indicates a bundle of wires. Intersections in the graph are not adders except solid circles. Delay elements and multipliers are randomly generated and connected, whose total is equal to the upper bound of chromosome length. Adders are naturally produced from the resulting structure. $x(n)$ and $y(n)$ are the input and the output of the system separately. There are 13 adders, 33 delay elements and 17 multipliers in it. The order of the filter is 9.

For comparison, four classic prototype filters are utilized to design IIR digital filters for the same desired filter. They are set in the same order of 9. The frequency responses without any fault are shown in Figure 4(a). All the design methods are meeting the design specification except Butterworth which fails to satisfy stopband attenuation at the cut off frequency of stopband.

Direct II, cascade, parallel and lattice structures are compared with our structure for fault tolerance. The prototype filters of Butterworth, Cheby I, Cheby II and Ellip are used. Each structure has 100 independent tests. Filter errors are composed of two parts, the error when the attenuation in passband is greater than 3 dB or less than 0 dB, and the error when the attenuation in stopband is less than 60 dB. Figure 4(b) illustrates the frequency response of five structures when they suffer a 1% mixed fault. Classic structure

implementations produce significant bias to the design specification except cascade form and the SEOA structure. In contrast to cascade form, SEOA gets a better adaption to faults.

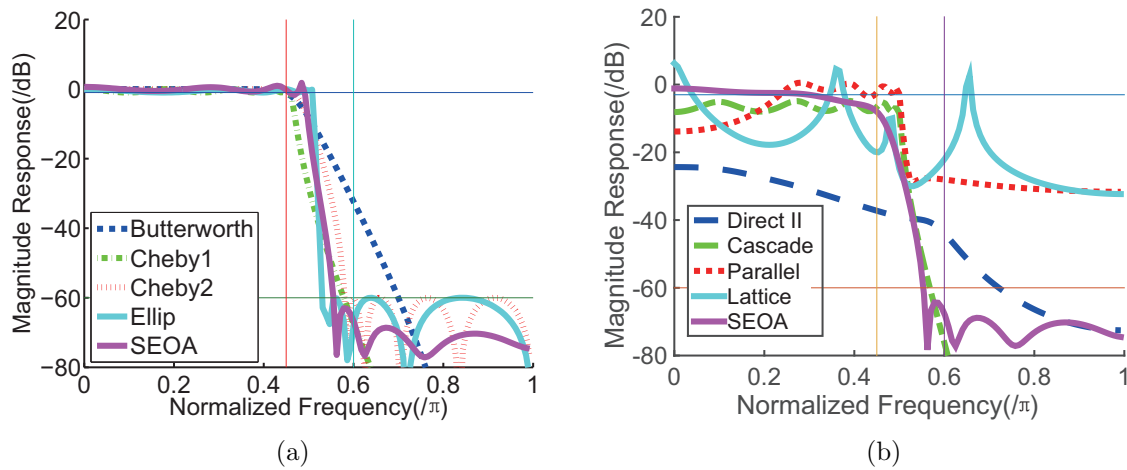


FIGURE 4. (a) The magnitude frequency responses using different prototype filters with the same order as our filter without any fault; (b) the magnitude frequency response comparison of our structure with four classic structures based on the Butterworth prototype filter at the mixed fault rate = 0.01

TABLE 2. Error comparison of four structures for implementing IIR digital low pass filters using different prototype filters with our structure (data in format: max(dB), mean(dB), var)

Fault rate	0.01	0.02	0.03	0.04	0.05
Butterworth					
Direct II	29/17/87	28/15/90	28/19/48	29/20/31	28/21/24
Cascade	<i>I/I/-</i>	<i>I/I/-</i>	<i>I/I/-</i>	<i>I/I/-</i>	<i>I/I/-</i>
Parallel	<i>B/92/B</i>	<i>B/95/B</i>	<i>B/B/B</i>	<i>I/I/-</i>	<i>I/I/-</i>
Lattice	28/16/83	30/22/42	31/25/27	32/25/24	32/26/20
Cheby I					
Direct II	26/10/20	24/19/10	25/19/14	24/20/11	26/20/10
Cascade	<i>I/I/-</i>	<i>I/I/-</i>	<i>I/I/-</i>	<i>I/I/-</i>	<i>I/I/-</i>
Parallel	27/21/41	<i>I/I/-</i>	<i>I/I/-</i>	<i>I/I/-</i>	<i>I/I/-</i>
Lattice	27/13/69	27/14/66	27/15/77	32/19/51	30/22/39
Cheby II					
Direct II	33/20/88	33/19/ <i>B</i>	32/20/ <i>B</i>	33/20/ <i>B</i>	33/24/35
Cascade	<i>I/I/-</i>	<i>I/I/-</i>	<i>I/I/-</i>	<i>I/I/-</i>	<i>I/I/-</i>
Parallel	<i>I/I/-</i>	<i>I/I/-</i>	50/39/68	<i>I/I/-</i>	<i>I/I/-</i>
Lattice	28/21/35	30/20/27	28/21/26	31/24/21	31/24/19
Elliptic					
Direct II	24/17/22	23/16/22	23/17/23	23 /16/24	23/17/22
Cascade	<i>I/I/-</i>	<i>I/I/-</i>	<i>I/I/-</i>	<i>I/I/-</i>	<i>I/I/-</i>
Parallel	<i>I/I/-</i>	27/22/36	<i>I/I/-</i>	<i>I/I/-</i>	<i>I/I/-</i>
Lattice	27/16/53	27/18/46	27/17/48	26/17/54	<i>I/I/-</i>
SEOA					
SEOA	16/6/13	19/9/14	21/9/14	23/11/15	22/11/14

Table 2 shows that the average trend of the errors is increasing when the fault rate increases from 1% to 5%. ‘I’ indicates an infinite number, ‘-’ indicates the result cannot be calculated and ‘B’ indicates a finite number greater than 100. The maximum, mean and variance of errors are compared using different structures in implementation of the filter in the table. The bold numbers indicate the smallest values at the same fault rate which is listed on the top of the same column. The maximum error and the mean error of SEOA are smallest in all structures. The error variance is at least second smallest among all structures. The results show that SEOA performs best among all methods when filter structures suffer mixed multiplier failures at the same fault rate.

4. Conclusion. In this letter, a design method for IIR low pass digital filters with fault tolerance is proposed, which can tolerate permanent mixed faults of multipliers. It is totally different from the traditional ones, which are often designed in a fixed pattern. Compared to the classic filter structures and design methods, the method can effectively improve fault tolerance.

The evolution of filter structures is a promising method to optimize filter structure characteristics. In the future, fault detection, fault tolerance and fault recover of digital filters based on this technique are valuable to be further investigated.

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