ICIC Express Letters
Volume **12**, Number **8**, August **2018**

 ISSN 1881-803X
pp. **815–822**

ANALYSIS OF BEAT FREQUENCY DETECTOR BASED ON BASIC LOGIC GATES

Anucha Kaewpoonsuk[1], Noppadon Sisuk[1], Krit Smerpitak[2] and Paramote Wardkein[2]

[1]Research Center for Academic Excellence in Applied Physics
Faculty of Science
Naresuan University
Phitsanulok 65000, Thailand
anuchak@nu.ac.th; noppadon_su@hotmail.com

[2]Faculty of Engineering
King Mongkut's Institute of Technology Ladkrabang
Chalongkrung Rd., Ladkrabang, Bangkok 10520, Thailand
krit.sm@kmitl.ac.th; promote@telecom.kmitl.ac.th

Received February 2018; accepted May 2018

Abstract. *The aim of this paper is to introduce a simple technique to analyze the operation of the basic logic gates-based beat frequency detector (BFD). We show that all of the basic logic gates, including AND-gate, NAND-gate, XOR-gate, XNOR-gate, OR-gate, and NOR-gate, can be used as a mixer to implement the BFD. This BFD is simple, easy to assemble, and can be used in control, instrument and measurement systems.*
Keywords: Beat frequency detector, Frequency difference detector, Logic gate, Mixer

1. **Introduction.** The basic idea of a beat frequency detector (BFD), also known as a frequency difference detector, is to generate an output signal with proportional frequency to the frequency difference of the two input signals. This circuit is very useful in control, instrument and measurement systems. For example, it can be used as the implement of the phase-locked-loop circuit [1-4], the modulator/demodulator [5-7], and the beat frequency oscillator metal detector [8-10]. Further references on their application can be found in [11-13]. There are two common approaches: sinusoidal wave signal processing and square wave signal processing to synthesize the BFD. The sinusoidal wave signal processing is either based on the analog multiplier circuit [14] or summing circuit [10]. However, it is a large complex structure with complicated operation. The square wave signal processing technique provides a simplified structure which is easier. In terms of conventional logic gates, an XOR gate or an NAND gate can be used to implement the BFD for square wave signal processing [5,6,15]. While a BFO metal detector was set up, beyond the XOR gate and the NAND gate, we found that the other basic logic gates are also used as a BFD. All devices employed with a low-pass filter can be used to implement a BFD. The interesting questions are listed as follows. Why is it so? How can we describe the relationship between the output and input square wave signals which have the difference frequencies? And what are similarity and difference due to using each basic logic gate? We have analyzed all the logic gate-based BFD operations based on the various rates of change of duty cycle [16] which require a diagram drawing of signals at different times for investigation. However, aforementioned methods are difficult to be analyzed. The aim of this paper is to present an alternative technique for analyzing the operation of basic logic gates-based BFD.

DOI: 10.24507/icicel.12.08.815

This paper is divided into 4 sections. We talk about the proposed application and design of the BFD. The XOR-gate and NAND-gate are widely used to implement the BFD as mentioned before. After that the other basic logic gates are analyzed to present that these can also be used as the BFD, described in Section 2. Details of experimental results and discussion are shown in Section 3. Finally, the conclusion and advantage obtained from analysis in this paper are in Section 4.

2. **Proposed Analysis Technique.** Table 1 shows the truth table of various basic logic gates. Taking the convenience into consideration, we start on the AND-gate which its duty is equivalent to the multiplication function since the other gates are more complicated. The circuit diagram of the BFD is shown in Figure 1. The assumption is if both input logic signals, Q_A and Q_B, of all logic gates are square wave voltages with 50% duty cycle, the Q_A and Q_B can be expanded as the Fourier series. The equation can be written as

$$Q_A = \frac{1}{2} + \frac{2}{\pi}\sum_{n=1}^{\infty}\frac{1}{n}\sin(n\omega_A t) \quad n = 1, 3, 5, \ldots \tag{1}$$

$$Q_B = \frac{1}{2} + \frac{2}{\pi}\sum_{m=1}^{\infty}\frac{1}{n}\sin(m\omega_B t) \quad m = 1, 3, 5, \ldots \tag{2}$$

where ω_A and ω_B are angular frequencies of Q_A and Q_B, respectively, and t is time.

Table 2 shows the equivalent functions of various basic logic gates. According to Table 2, the output logic of AND-gate is equivalent to the multiplication of both input logics. Substituting the output signal $Q_{G(\mathrm{AND})}$ of AND-gate by the multiplication of two

TABLE 1. Truth table of various basic logic gates

Input		Output					
Q_A	Q_B	AND-gate	NAND-gate	NOR-gate	OR-gate	XOR-gate	XNOR-gate
0	0	0	1	1	0	0	1
0	1	0	1	0	1	1	0
1	0	0	1	0	1	1	0
1	1	1	0	0	1	0	1

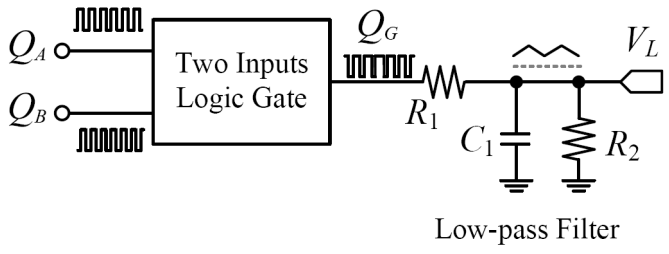


FIGURE 1. Beat frequency detector based on two input logic gates

TABLE 2. Equivalent functions of various basic logic gates

Gate Types	Equivalent Functions
AND gate	$Q_{G(\mathrm{AND})} = Q_A Q_B$
NAND gate	$Q_{G(\mathrm{NAND})} = 1 - Q_A Q_B = 1 - Q_{G(\mathrm{AND})}$
OR gate	$Q_{G(\mathrm{OR})} = 1 - \{(1 - Q_A)(1 - Q_B)\} = 1 - Q_{G(\mathrm{NOR})}$
NOR gate	$Q_{G(\mathrm{NOR})} = (1 - Q_A)(1 - Q_B)$
XOR gate	$Q_{G(\mathrm{XOR})} = 1 - \{(Q_A Q_B) + (1 - Q_A)(1 - Q_B)\} = 1 - Q_{G(\mathrm{XNOR})}$
XNOR gate	$Q_{G(\mathrm{XNOR})} = Q_A Q_B + (1 - Q_A)(1 - Q_B)$

continuous square waves with different frequencies from (1) and (2), we get

$$Q_{G(\mathrm{AND})} = Q_A Q_B = \left(\frac{1}{2} + \frac{2}{\pi}\sum_{n=1}^{\infty}\frac{1}{n}\sin(n\omega_A t)\right)\left(\frac{1}{2} + \frac{2}{\pi}\sum_{m=1}^{\infty}\frac{1}{m}\sin(m\omega_B t)\right) \tag{3}$$

Equation (3) can be expanded as

$$\begin{aligned} Q_{G(\mathrm{AND})} = &\frac{1}{4} + \frac{1}{\pi}\sum_{n=1}^{\infty}\frac{1}{n}\sin(n\omega_A t) + \frac{1}{\pi}\sum_{m=1}^{\infty}\frac{1}{m}\sin(m\omega_B t) \\ &+ \frac{4}{\pi^2}\sum_{n=1}^{\infty}\sum_{m=1}^{\infty}\frac{1}{nm}\sin(n\omega_A t)\sin(m\omega_B t) \end{aligned} \tag{4}$$

From a trigonometric identity,

$$\sin A \sin B = \frac{1}{2}\cos(A-B) - \frac{1}{2}\cos(A+B) \tag{5}$$

the fourth term on the right-hand side of Equation (4) can be written as

$$\begin{aligned} &\sum_{n=1}^{\infty}\sum_{m=1}^{\infty}\frac{1}{nm}\sin(n\omega_A t)\sin(m\omega_B t) \\ &= \sum_{n=1}^{\infty}\sum_{m=1}^{\infty}\frac{1}{nm}\left[\frac{1}{2}\cos(n\omega_A - m\omega_B)t - \frac{1}{2}\cos(n\omega_A + m\omega_B)t\right] \end{aligned} \tag{6}$$

By substituting Equation (6) into Equation (4), we get

$$\begin{aligned} Q_{G(\mathrm{AND})} = &\frac{1}{4} + \frac{1}{\pi}\sum_{n=1}^{\infty}\frac{1}{n}\sin(n\omega_A t) + \frac{1}{\pi}\sum_{m=1}^{\infty}\frac{1}{m}\sin(m\omega_B t) \\ &+ \frac{2}{\pi^2}\sum_{n=1}^{\infty}\sum_{m=1}^{\infty}\frac{1}{nm}\left[\cos(n\omega_A - m\omega_B)t\right] \\ &- \frac{2}{\pi^2}\sum_{n=1}^{\infty}\sum_{m=1}^{\infty}\frac{1}{nm}\left[\cos(n\omega_A + m\omega_B)t\right] \end{aligned} \tag{7}$$

If considering the fourth term in the right-hand of Equation (7), let $\omega_A = \omega_B + \Delta\omega$, Equation (7) becomes

$$\begin{aligned} Q_{G(\mathrm{AND})} = &\frac{1}{4} + \frac{1}{\pi}\sum_{n=1}^{\infty}\frac{1}{n}\sin(n\omega_A t) + \frac{1}{\pi}\sum_{m=1}^{\infty}\frac{1}{m}\sin(m\omega_B t) \\ &+ \frac{2}{\pi^2}\sum_{n=1}^{\infty}\sum_{m=1}^{\infty}\frac{1}{nm}\left[\cos((n-m)\omega_B t + n\Delta\omega t)\right] \\ &- \frac{2}{\pi^2}\sum_{n=1}^{\infty}\sum_{m=1}^{\infty}\frac{1}{nm}\left[\cos(n\omega_A + m\omega_B)t\right] \end{aligned} \tag{8}$$

It can be assumed that $V_{L(\mathrm{AND})}$ is the ideal output signal of a low-pass filter with $Q_{G(\mathrm{AND})}$ input signal. Since the variables n and m are the odd integer, we assume that if $\omega_B >> \Delta\omega$, then the high frequency components of $V_{L(\mathrm{AND})}$ are eliminated in case of $n \neq m$. Equation (8) can be approximated as

$$V_{L(\mathrm{AND})} = \frac{1}{4} + \frac{2}{\pi^2}\sum_{i=1}^{\infty}\frac{1}{i^2}\left[\cos(i\Delta\omega t)\right] \tag{9}$$

where $i = n = m = 1, 2, 3, \ldots$.

From Equation (9), note that the angular frequency of the triangular waveform signals are equal to $\Delta\omega = |\omega_A - \omega_B|$. Moreover, the values of the DC component that is equal to a quarter of logic "1" at voltage level of AND-gate output signal are also included in these signals. In the following step, NOR-gate is considered. From Table 2, the output voltage signal of NOR-gate is equivalent to a function:

$$Q_{G(\mathrm{NOR})} = (1 - Q_A)(1 - Q_B) = 1 - Q_A - Q_B + Q_A Q_B \tag{10}$$

Substituting the Q_A and Q_B (Equations (1) and (2)) into Equation (10), we get

$$\begin{aligned} Q_{G(\mathrm{NOR})} = \frac{1}{4} &- \frac{1}{\pi}\sum_{n=1}^{\infty}\frac{1}{n}\sin(n\omega_A t) - \frac{1}{\pi}\sum_{m=1}^{\infty}\frac{1}{m}\sin(m\omega_B t) \\ &+ \frac{4}{\pi^2}\sum_{n=1}^{\infty}\frac{1}{n}\sin(n\omega_A t)\sum_{m=1}^{\infty}\frac{1}{m}\sin(m\omega_B t) \end{aligned} \tag{11}$$

Similar to Equation (4), by applying $Q_{G(\mathrm{NOR})}$ to low-pass filter, we get the output signal $V_{L(\mathrm{NOR})}$ of such low-pass filter as

$$V_{L(\mathrm{NOR})} = \frac{1}{4} + \frac{2}{\pi^2}\sum_{i=1}^{\infty}\frac{1}{i^2}\left[\cos(i\Delta\omega t)\right] \tag{12}$$

XNOR-gate is the third device that we considered. From Table 2, the output voltage signal of XNOR-gate is equivalent to the function as

$$Q_{G(\mathrm{XNOR})} = Q_A Q_B + (1 - Q_A)(1 - Q_B) = 1 - Q_A - Q_B + 2Q_A Q_B \tag{13}$$

Substituting the signals Q_A and Q_B (Equations (1) and (2)) into Equation (13), it gives

$$Q_{G(\mathrm{XNOR})} = \frac{1}{2} + \frac{8}{\pi^2}\sum_{n=1}^{\infty}\frac{1}{n}\sin(n\omega_A t)\sum_{m=1}^{\infty}\frac{1}{m}\sin(m\omega_B t) \tag{14}$$

This equation is similar to Equations (4) and (11); after $Q_{G(\mathrm{XNOR})}$ is applied to low-pass filter, the output signal $V_{L(\mathrm{XNOR})}$ of the low-pass filter is

$$V_{L(\mathrm{XNOR})} = \frac{1}{2} + \frac{4}{\pi^2}\sum_{i=1}^{\infty}\frac{1}{i^2}\left[\cos(i\Delta\omega t)\right] \tag{15}$$

Finally, the NAND-gate, OR-gate and XOR-gate which are the inverse functions of AND-gate, NOR-gate and XNOR-gate are also considered, respectively. From Table 2, the output voltage signals of NAND-gate, OR-gate and XOR-gate are equivalent to the function, respectively.

$$Q_{G(\mathrm{NAND})} = 1 - Q_A Q_B = 1 - Q_{G(\mathrm{AND})} \tag{16}$$

$$Q_{G(\mathrm{OR})} = 1 - (1 - Q_A)(1 - Q_B) = 1 - Q_{G(\mathrm{NOR})} \tag{17}$$

$$Q_{G(\mathrm{XOR})} = 1 - Q_A Q_B + (1 - Q_A)(1 - Q_B) = 1 - Q_{G(\mathrm{XNOR})} \tag{18}$$

In addition, results of the experiment and mathematical analysis show that the circuits designed using the XOR-gate and XNOR-gate provide the triangular output signal which has the biggest amplitude. Then, both two logic gates are more suitable for the applying than the other logic gates unless the circuit designers desire to build the oscillator and BFD with the same type of the logic gate. The NAND-gate and NOR-gate are suitable to use in this case. Similarly to the first three gates, substituting the signals Q_A and Q_B (Equations (1) and (2)) in Equations (16), (17) and (18) and using characteristic of the low-pass filter, the output voltage signals of circuit are determined, respectively as

$$V_{L(\mathrm{NAND})} = \frac{3}{4} - \frac{2}{\pi^2}\sum_{i=1}^{\infty}\frac{1}{i^2}\left[\cos(i\Delta\omega t)\right] \tag{19}$$

$$V_{L(\mathrm{OR})} = \frac{3}{4} - \frac{2}{\pi^2}\sum_{i=1}^{\infty}\frac{1}{i^2}\left[\cos(i\Delta\omega t)\right] \tag{20}$$

$$V_{L(\mathrm{XOR})} = \frac{1}{2} - \frac{4}{\pi^2}\sum_{i=1}^{\infty}\frac{1}{i^2}\left[\cos(i\Delta\omega t)\right] \tag{21}$$

From Equations (9), (12), (15) and (19)-(21), the triangular signals $V_{L(\mathrm{AND})}$ and $V_{L(\mathrm{NOR})}$ are in phase, but they are out of phase with signals $V_{L(\mathrm{NAND})}$ and $V_{L(\mathrm{OR})}$. The DC output voltages of signals $V_{L(\mathrm{AND})}$ and $V_{L(\mathrm{NOR})}$ are quarter of logic "1"-voltage level of the gates while the DC output voltages of signals $V_{L(\mathrm{NAND})}$ and $V_{L(\mathrm{OR})}$ are three quarter of logic "1"-voltage level of the gates. The signals $V_{L(\mathrm{XNOR})}$ and $V_{L(\mathrm{XOR})}$ have the larger magnitudes which are equal to the half of logic "1"-voltage level of the gates, but both signals are out of phase.

3. **Experimental Results and Discussions.** For experimental purposes, the circuit of Figure 1 using a variety of basic logic gates was constructed on a bread board. The supply voltage used is 5 V. The commercially available transistor-transistor logic (TTL) devices including 74ls08, 74ls00, 74ls32, 74ls02, and 74ls46 were used to test as the AND-gate, NAND-gate, OR-gate, NOR-gate, and XOR-gate, respectively. The XNOR-gate, 74ls46, was used together with NOT-gate, 74ls04. The frequency of TTL signal Q_A is 100 kHz.

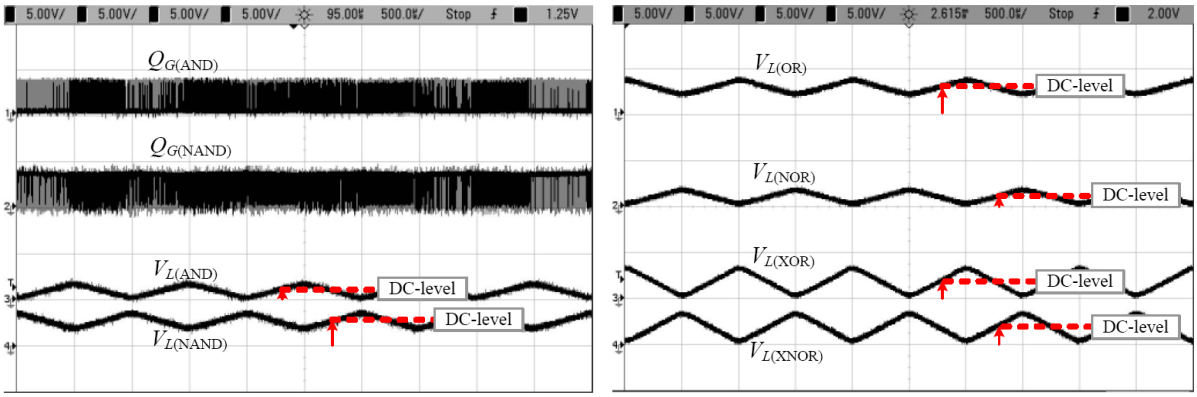


FIGURE 2. Measured results by applying Q_A and Q_B having frequency of 100 kHz and 101 kHz, respectively (Vertical scale: 5 V/div., horizontal scale: 0.5 ms/div.)

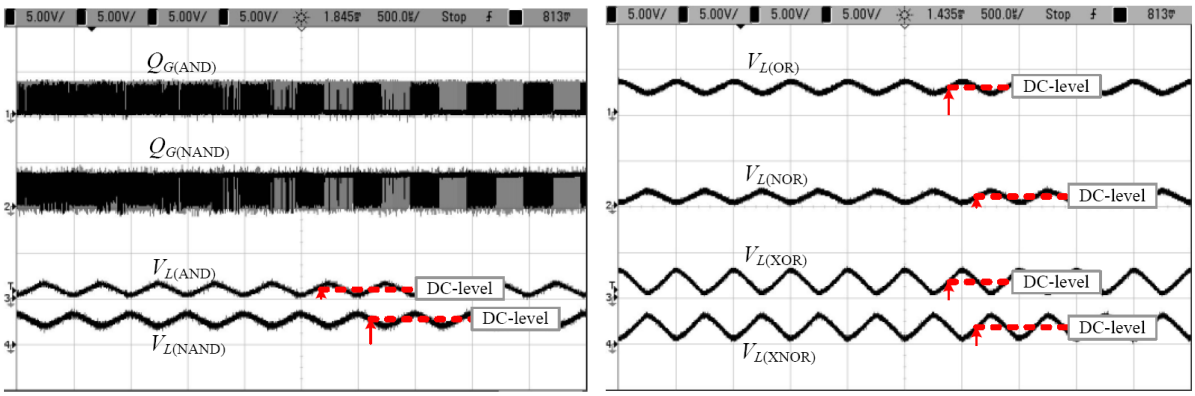


FIGURE 3. Measured results by applying Q_A and Q_B having frequency of 100 kHz and 102 kHz, respectively (Vertical scale: 5 V/div., horizontal scale: 0.5 ms/div.)

The values of components were chosen as $R_1 = 1$ kΩ, $R_2 = 1$ MΩ, and $C_1 = 10$ nF. Hence, the cutoff frequency at 15.9 kHz of low-pass filter can be achieved.

Figures 2, 3 and 4 show the measured results for various frequencies of TTL signal Q_B which are 101 kHz, 102 kHz, and 103 kHz, respectively. Note that all the output signals have frequency equal to the frequency difference between Q_A and Q_B signals. In Figure 2, the frequencies of the triangular output signals $V_{L(\mathrm{AND})}$, $V_{L(\mathrm{NAND})}$, $V_{L(\mathrm{OR})}$, $V_{L(\mathrm{NOR})}$,

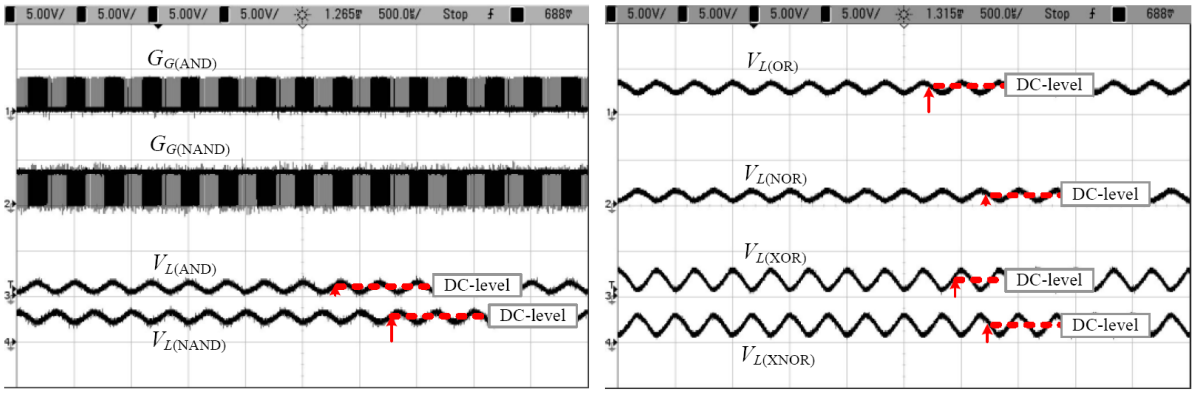
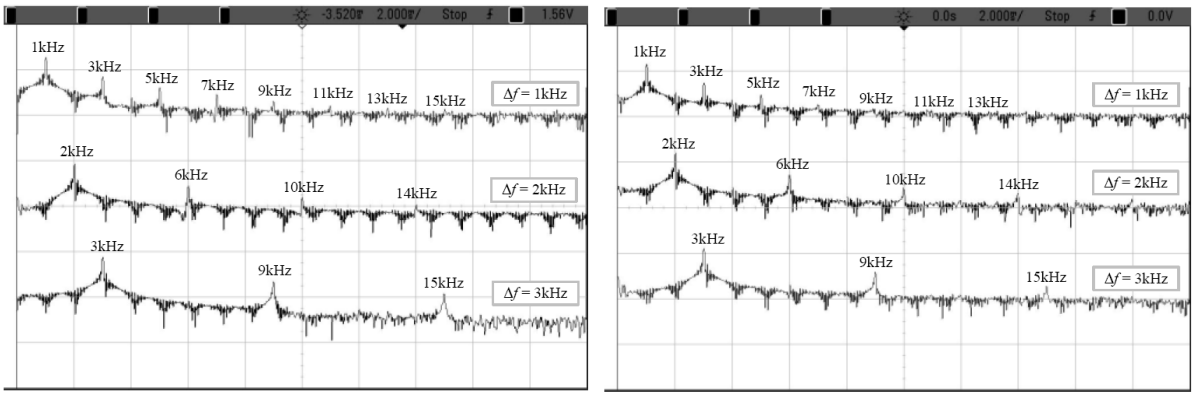
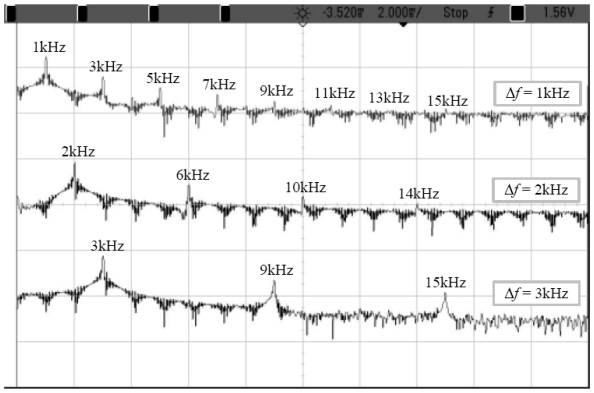


FIGURE 4. Measured results by applying Q_A and Q_B having frequency of 100 kHz and 103 kHz, respectively (Vertical scale: 5 V/div., horizontal scale: 0.5 ms/div.)



(a) AND gate

(b) OR gate



(c) XOR gate

FIGURE 5. Spectrum analysis of signals $V_{L(\mathrm{AND})}$, $V_{L(\mathrm{OR})}$ and $V_{L(\mathrm{XOR})}$ for varying the input frequency difference (Δf) (Vertical scale: 50 dB/div., horizontal scale: 2 kHz/div.)

$V_{L(\mathrm{XOR})}$ and $V_{L(\mathrm{XNOR})}$ are equal to 1 kHz. Similarly, the triangular output signals of all the logic gates as shown in Figures 3 and 4 have the frequencies which are equal to 2 kHz and 3 kHz, respectively. Moreover, the measured DC levels of all output signals are compliant with the analyzed values.

Figure 5 shows the spectrum analysis of signals $V_{L(\mathrm{AND})}$, $V_{L(\mathrm{OR})}$ and $V_{L(\mathrm{XOR})}$ for varying the input frequency difference. There are evidences that all the output signals comprise the fundamental frequency particularly the odd frequency components, that is, the special characteristic of the triangular waveforms with frequency equal to the fundamental frequency.

4. **Conclusions.** Analysis of beat frequency detector based on two-input basic logics is previously demonstrated. The analytic approach for both square input signals of logic gates can be represented as the Fourier series. Then, they can be operated by the mathematical operators which are equivalent to duty of each logic gate. The experimental results reveal that the outputs of each logic gates are the triangular waveform signals with variation of DC components. Corresponding to the analysis results, all the triangular waveform signals have the angular frequencies equal to the frequency difference of two input signals. Furthermore, the DC-voltage components achieved by analysis in this paper are useful for application in circuit designs such as the converting from the triangular output signal to the square wave signal for driving loads. It can be operated simply by using the comparator which has the amplitude of a reference signal which is equal to the DC-voltage level of the triangular output signal of each logic gate.

REFERENCES

[1] B. H. Nagpara and R. S. Gajre, Design, implementation and analysis of digital phase locked loop using XOR phase detector in 50 nm CMOS technology, *Int. J. Adv. Engineering & Application*, pp.130-133, 2011.

[2] D. Harikrushna, M. Tiwari, J. K. Singh and A. Khare, Design, implementation and characterization of XOR phase detector for DPLL in 45 nm CMOS technology, *Int. J. Adv. Comput.*, vol.2, no.6, pp.45-57, 2011.

[3] M. Kumar and K. Lata, FPGA implementation of ADPLL with ripple reduction techniques, *Int. J. VLSI Design Commun. Syst.*, vol.3, no.2, pp.99-106, 2012.

[4] V. Prasad and C. Sharma, A review of phase locked loop, *Int. J. Emerging Technol. Adv. Eng.*, vol.2, no.6, pp.98-104, 2012.

[5] K. Wortel, L. J. Briones and T. L. Stockstad, FSK modulator using IQ up-mixers and sine wave coder ACS, *U.S. Patent, US007043222B2*, 2006.

[6] E. Kabalci and Y. Kabalci, A measurement and power line communication system design for renewable smart grids, *Meas. Sci. Rev.*, vol.13, no.5, pp.248-252, 2013.

[7] L. Xu, L. Sun and X. Hu, Design and realization of a UHF RFID interrogator, *Int. J. Smart Sens. Intell. Syst.*, vol.6, no.3, pp.1012-1030, 2013.

[8] K. D. Skeldon, L. M. Reid, V. McInally, B. Dougan and C. Fulton, Physics of the Theremin, *Am. J. Phys.*, vol.66, no.11, pp.945-955, 1998.

[9] *A Simple Metal Detector Circuit Using Beat Frequency Oscillator*, Resource Document, http://www.hqew.net/circuit-diagram/A-Simple-Metal-Detector-Circuit-Using-Beat-Frequency-Oscillator-(BFO)_2719.html, 2012.

[10] C. Youssef, B. R. Mohamed, A. Najmeddine, T. Frikha and W. Jmal, Mine detecting robot prototyping, *Proc. of Int. Conf. on Anti-Cyber Crimes (ICACC)*, Saudi Arabia, 2017.

[11] V. Štofanik, V. Vretenár and V. Boháč, Compensation of systematic error due to sampling rate versus temperature dependency utilizing a dual-mode crystal oscillator, *Measurement Science Review*, vol.5, no.1, pp.52-55, 2005.

[12] A. De Marcellis and G. Ferri, Analog circuits and systems for voltage-mode and current-mode sensor, *Interfacing Applications*, pp.185-188, 2011.

[13] A. Boua and J. Kroutil, Precise beat frequency evaluation circuit for multi-oscillators QCM gas detectors, *Proc. of the 10th Int. Conf. Advanced Semiconductor Devices and Microsystem*, Salovakia, 2014.

[14] G. A. Leonov, N. V. Kuznetsov, M. V. Yuldashev and R. V. Yuldashev, Analytical method for computation of phase-detector characteristic, *IEEE Trans. Circuit Syst. II: Express Briefs*, vol.59, no.10, pp.633-637, 2012.

[15] K. Prompak, A. Kaewpoonsuk, T. Maneechukate, W. Phanphaisarn and P. Wardkein, Flow rate controlling using phase-locked loop, *ICIC Express Letters*, vol.7, no.3(A), pp.753-758, 2013.

[16] A. Kaewpoonsuk, Basic logic circuits in realizing differencing frequency detector for beat-frequency-oscillator-based metal detector, *Int. J. King Mongkut's University of Technology North Bangkok*, vol.21, no.1, pp.41-51, 2011.