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VOLTAGE CHARACTERISTICS OF A HAMMING DISTANCE SEARCH CIRCUIT IN VOLTAGE DOMAIN USING CLOCKED NEURON CMOS INVERTER

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Abstract. *A time domain Hamming distance search circuit using a clocked neuron CMOS inverter with a current mirror has been reported. This circuit searches Hamming distance between two input data by using time domain. For this reason, the conventional circuit takes time to search the Hamming distance. In this paper, we propose a Hamming distance search circuit using voltage domain for a content addressable memory. The proposed circuit searches the Hamming distance by the floating gate voltage of the clocked neuron CMOS inverter. Therefore, the proposed circuit can search faster than the conventional circuit. Furthermore, we analyze and simulate the voltage characteristics of the proposed circuit using 0.18μm CMOS process of ROHM Semiconductor with HSPICE, and clarify the usefulness of the proposed circuit.*
Keywords: Hamming distance, CAM, Neuron CMOS inverter, Voltage domain

1. **Introduction.** Recently, AI (Artificial Intelligence) and big data have attracted a lot of attention and are studied and developed actively. In this field, a large amount of data is read out, written and calculated. Also, the development of memory-driven computing, which increases processing speed by focusing on memory, has been started [1,2]. As a result, there is an increasing of importance of a high-speed memory.

A Content Addressable Memory (CAM) is useful for processing a large amount of data, because it can perform a high-speed search in fully parallel [3,4]. The CAM which performs a flexible search using Hamming distance with a clocked neuron CMOS inverter has been reported [5]. However, there is a problem that an accurate search cannot be performed, because the initial charge of the floating gate of the clocked neuron CMOS inverter is unstable.

This problem was solved by the Hamming distance detector in a time domain using the current mirror which keeps a constant current [6,7]. However, the time domain search of this circuit takes a long time, because the circuit detects the Hamming distance by a

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time difference. Furthermore, in this circuit, calibration operation is necessary every time after completion of the searching by the current mirror.

In this paper, we propose a fast and flexible search circuit which does not use the current mirror. In the proposed circuit, the calibration operation is performed by using the characteristics that the floating gate voltage becomes equal to the inversion threshold voltage by connecting the input terminal and the output terminal of the inverter. The proposed circuit makes the decision by using the floating gate voltage of the clocked neuron CMOS inverter, and performs a Hamming distance search using the voltage domain. In this paper, we analyze and simulate the voltage characteristics of the proposed circuit using 0.18μm CMOS process of ROHM Semiconductor with HSPICE. First, we show the configuration and operation of the conventional circuit and point out the problems. In Chapter 3, the configuration and operation principle of the proposed circuit will be described. In Chapter 4, we compare the proposed circuit and the conventional circuit from HSPICE simulations. Chapter 5 summarizes this paper.

2. **Structure of Conventional Circuit and Problems.** The conventional circuit using the current mirror is shown in Figure 1(a). This circuit measures the Hamming distance between two input data DATA-A$(a_1, a_2, a_3, \ldots, a_n)$ and DATA-B$(b_1, b_2, b_3, \ldots, b_n)$. Here, n is the bit length. The conventional circuit is composed of three parts: an XOR gate array for checking whether each bit matches, a clocked neuron CMOS inverter for making a decision, and a current mirror used for flowing a constant current. The operation of the circuit is shown in Figure 1(b). As shown in this figure, the Hamming distance search can be performed by controlling 5 stages of each transistor.

Each operation will be explained. In Phase 1, the calibration operation that is set the floating gate voltage $V(G_F)$ of the clocked neuron CMOS inverter to the inversion threshold voltage V_{INV} is performed. In Phase 2, the calibration is stopped. In Phase 3, the $V(G_F)$ is adjusted to allow Hamming distance to be judged. In Phase 4, an exact match search is performed. Finally, in Phase 5, the conventional circuit performs

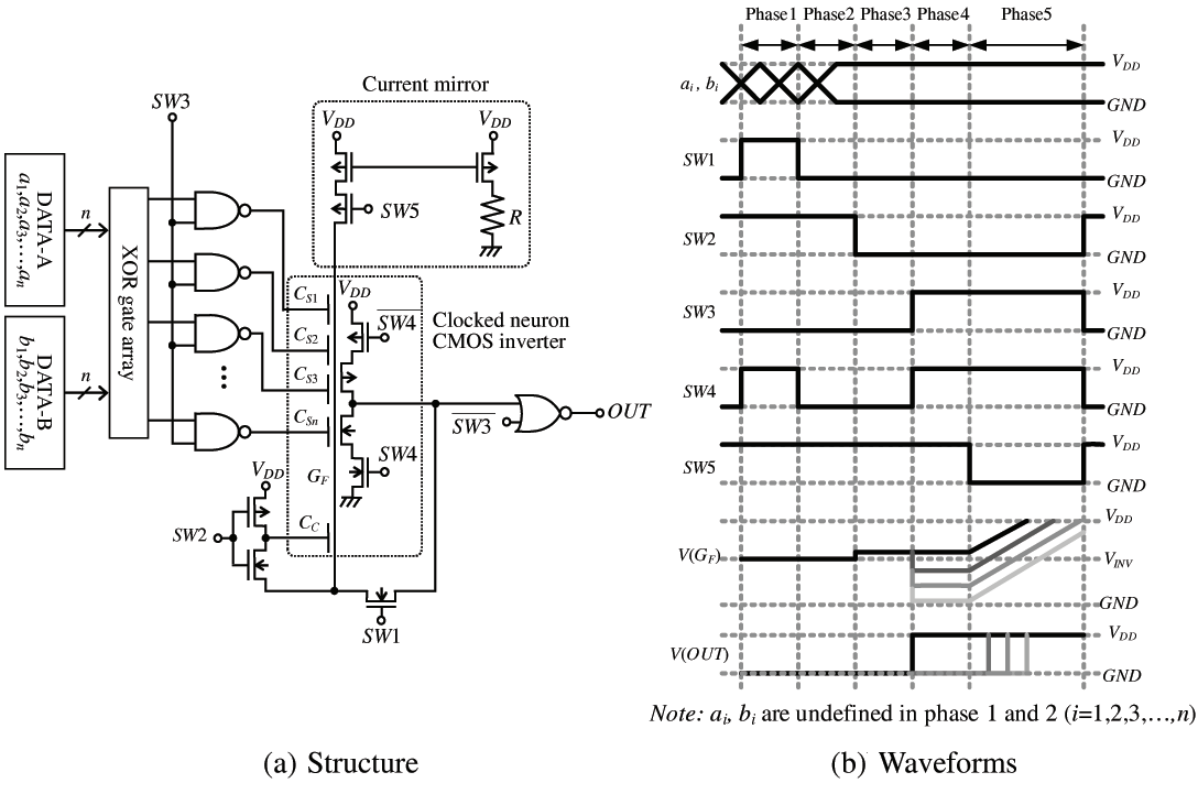


FIGURE 1. Circuit configuration and waveform of conventional circuit

Hamming distance search. In this way, the conventional circuit can perform flexible Hamming distance search. However, the conventional circuit takes time to search for the Hamming distance, because the circuit searches using the time difference by the current mirror at Phase 5. In Chapter 3, we propose a Hamming distance search circuit using the voltage domain that does not use the current mirror. The proposed circuit searches using the magnitude relation between the value of the floating gate voltage and the inversion threshold voltage of the clocked neuron CMOS inverter.

3. Configuration and Operation of the Proposed Circuit.

3.1. Circuit configuration.

The proposed circuit is shown in Figure 2(a). The proposed circuit consists of an XOR gate array for measuring whether each bit of two data matches, a reference distance setting circuit for setting the reference distance, and a clocked neuron CMOS inverter for making a judgment.

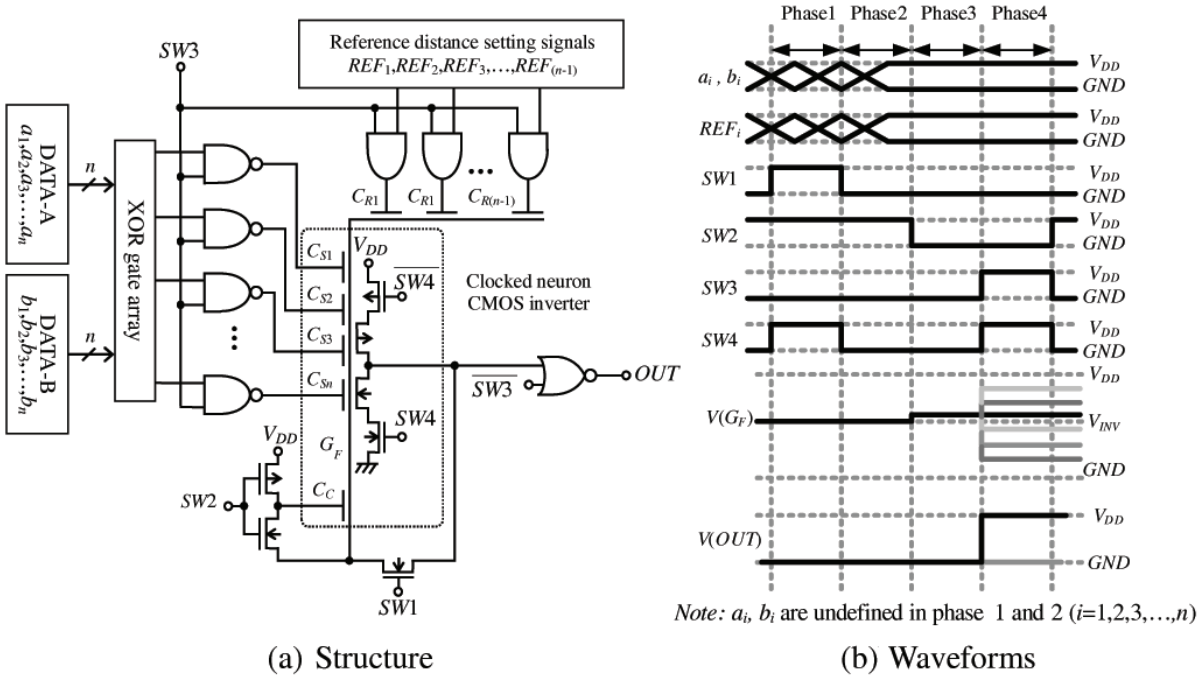


FIGURE 2. Circuit configuration and waveform of the proposed circuit

The circuit measures the Hamming distance of two data DATA-A$(a_1, a_2, \ldots, a_i, \ldots, a_n)$ and DATA-B$(b_1, b_2, \ldots, b_i, \ldots, b_n)$, judging whether the Hamming distance is within the reference distance or not. This proposed circuit performs a searching operation using four control signals. $SW1$ is a signal for controlling NMOS for making the value of the floating gate voltage $V(G_F)$ equal to the inversion threshold voltage of the clocked neuron CMOS inverter. $SW2$ is a signal for controlling two MOS transistors, and set the voltage of the floating gate to a value slightly higher than the inversion threshold voltage. $SW3$ is a signal for setting initial states of AND, NAND, and NOR circuits. $SW4$ is a control signal for setting the operation state of the clocked neuron CMOS inverter.

This circuit sets reference distance to perform an in-range search by reference distance setting signals REF_i $(i = 1, 2, \ldots, n-1)$. Also, the proposed circuit has n capacitors for measuring the Hamming distance, $n-1$ capacitors for setting the reference distance, and one capacitor used for forming the initial state. As a result, the total number of capacitors is $2n$. The capacitances of all the capacitors of the proposed circuit are assumed to be equal.

$$C_C = C_{S1} = C_{S2} = \cdots = C_{Sn} = C_{R1} = C_{R2} = \cdots = C_{R(n-1)}. \quad (1)$$

3.2. **Operation principles.** The movement of each control signal and the ideal operation of the output at that time are shown in Figure 2(b). As shown in this figure, the proposed circuit performs the search operation by manipulating the respective control signals with four phases. Also, in the initial state of each control signal, it is assumed that $SW1$, $SW3$, $SW4$ are GND and $SW2$ is the power supply voltage V_{DD}.

3.2.1. *Calibration operation.* In Phase 1, the calibration operation is performed by raising the control signals $SW1$ and $SW4$ from GND to V_{DD}. Then, the output terminal and the input terminal of the clocked neuron CMOS inverter are connected. At this time, assuming that the inversion threshold voltage of the clocked neuron CMOS inverter is V_{INV}, the floating gate voltage $V(G_F)$ is equal to V_{INV}. Therefore, the floating gate voltage $V(G_F)$ when performing the calibration is expressed as the following equation.

$$V(G_F) \mid_{\text{Phase1}} = V_{INV}. \tag{2}$$

The inversion threshold voltage V_{INV} of the proposed circuit is designed to half of V_{DD}. By keeping $SW3$ at GND in this phase, the applied voltage to the total $2n-1$ capacitors for the Hamming distance measurement and the reference distance setting become V_{DD} and GND.

In Phase 2, $SW1$ and $SW4$ are set from V_{DD} to GND, and the input and the output of the clocked neuron CMOS inverter are disconnected. At this time, the voltage $V(C_C)$ applied to C_C is represented by

$$V(C_C) = V_{INV}. \tag{3}$$

3.2.2. *Adjustment of floating gate voltage.* In Phase 3, in order to make a decision operation, the floating gate voltage is changed from the inversion threshold voltage of the clocked neuron CMOS inverter to a value slightly higher than that by lowering $SW2$ from V_{DD} to GND. By changing the voltage of $SW2$, $V(C_C)$ becomes

$$V(C_C) = V_{DD}. \tag{4}$$

The change amount of the floating gate voltage at this time is

$$\Delta V(G_F) \mid_{\text{Phase3}} = \frac{C_C}{C_{TOT}} \Delta V(C_C) = \frac{C_C}{C_{TOT}} (V_{DD} - V_{INV}) = \frac{C_C}{C_{TOT}} \cdot \frac{V_{DD}}{2}, \tag{5}$$

where C_{TOT} in each equation is

$$C_{TOT} = C_{S1} + C_{S2} + \cdots + C_{Sn} + C_{R1} + C_{R2} + \cdots + C_{R(n-1)} + C_C. \tag{6}$$

Therefore, the floating gate voltage becomes

$$\begin{aligned} V(G_F) \mid_{\text{Phase3}} &= V(G_F) \mid_{\text{Phase1}} + \Delta V(G_F) \mid_{\text{Phase3}} \\ &= V_{INV} + \frac{C_C}{C_{TOT}} \cdot \frac{V_{DD}}{2} = V_{INV} + \frac{1}{2n} \cdot \frac{V_{DD}}{2}. \end{aligned} \tag{7}$$

This equation shows that the floating gate voltage is higher than the inversion threshold voltage of the clocked neuron CMOS inverter. Also, three inputs a_i $(i = 1, 2, 3, \ldots, n)$, b_i $(i = 1, 2, 3, \ldots, n)$, REF_i $(i = 1, 2, 3, \ldots, n-1)$ must be determined in Phase 3.

3.2.3. *Search Hamming distance.* Here, it is assumed that 0[V] is input to all the reference distance setting signals. Phase 4 uses XOR gate arrays to search for Hamming distance by setting $SW3$ and $SW4$ to V_{DD}. In this phase, depending on the result of the XOR gate array, the applied voltage to each capacitor becomes V_{DD} if a bit of DATA-A and DATA-B is in agreement. On the other hand, the voltage becomes GND respectively if a mismatch occurs. Here, when Hamming distance between DATA-A$(a_1, a_2, \ldots, a_i, \ldots, a_n)$ and DATA-B$(b_1, b_2, \ldots, b_i, \ldots, b_n)$ is D_{HS}, it becomes

$$D_{HS} = \sum_{i=1}^{n} (a_i \oplus b_i). \tag{8}$$

When the Hamming distance D_{HS} between DATA-A and DATA-B is 0, the floating gate voltage $V(G_F)$ does not change from the state of Phase 3. Therefore, in this case, the $V(G_F)$ is expressed as

$$V(G_F) \mid_{\text{Phase4}} = V(G_F) \mid_{\text{Phase3}} = V_{INV} + \frac{1}{2n} \cdot \frac{V_{DD}}{2}. \tag{9}$$

When the Hamming distance D_{HS} is 1 or more, the floating gate voltage $V(G_F)$ decreases stepwise according to D_{HS}. Assuming that the change amount of the floating gate voltage by D_{HS} is $\Delta V(G_F, D_{HS})$, it becomes

$$\Delta V(G_F, D_{HS}) = -\frac{D_{HS}}{2n} \cdot V_{DD}. \tag{10}$$

Therefore, the floating gate voltage $V(G_F)$ in consideration of this change amount is expressed as:

$$V(G_F) \mid_{\text{Phase4}} = V_{INV} + \frac{1}{2n} \cdot \frac{V_{DD}}{2} - \frac{D_{HS}}{2n} \cdot V_{DD} = V_{INV} - \frac{2D_{HS} - 1}{2n} \cdot \frac{V_{DD}}{2}. \tag{11}$$

3.2.4. *Operation when reference distance is set.* In addition to exact match search, the proposed circuit is also possible to perform a fuzzy search that sets the reference distance D_{HR} and searches for data within the specified range. In the operation of the proposed circuit, performing the fuzzy search can be realized by inputting the reference distance setting signals according to Table 1 before the step of entering Phase 4.

Table 1. Reference distance

D_{HR}	REF_1	REF_2	$\cdots$	$REF_{(n-1)}$
0	0[V]	0[V]	$\cdots$	0[V]
1	V_{DD}	0[V]	$\cdots$	0[V]
2	V_{DD}	V_{DD}	$\cdots$	0[V]
$\vdots$			$\ddots$	
$n-1$	V_{DD}	V_{DD}	$\cdots$	V_{DD}

At this time, the floating gate voltage increases step by step with the specified reference distance setting signals. When the change amount of the floating gate voltage at this time is $\Delta V(G_F, D_{HR})$, it becomes

$$\Delta V(G_F, D_{HR}) = \frac{D_{HR}}{2n} \cdot V_{DD}. \tag{12}$$

It can be seen from Equation (9) that amount of increase of the floating gate voltage is equal to the amount of decrease according to the Hamming distance D_{HS}. Therefore, from (11) and (12), the floating gate voltage $V(G_F)$ in consideration of the reference distance setting signal is expressed by

$$\begin{aligned} V(G_F) \mid_{\text{Phase4}} &= V(G_F) \mid_{\text{Phase3}} + \Delta V(G_F, D_{HS}) + \Delta V(G_F, D_{HR}) \\ &= V_{INV} + \frac{2D_{HR} - 2D_{HS} + 1}{2n} \cdot \frac{V_{DD}}{2}. \end{aligned} \tag{13}$$

Therefore, when D_{HS} is larger than the reference distance D_{HR}, the output voltage $V(OUT)$ becomes 0[V], and when D_{HS} equal to or less than D_{HR}, it becomes V_{DD}.

In this way, the proposed circuit performs operations from Phase 1 to Phase 4, and detects the Hamming distance between DATA-A and DATA-B. In Phase 4, search time can be shortened, because there is no current mirror and the determination is made only with the voltage of the floating gate. The floating gate voltage of Phase 4 is shown in Figure 3, where the reference distance $D_{HR} = 0$. The proposed circuit performs search operation

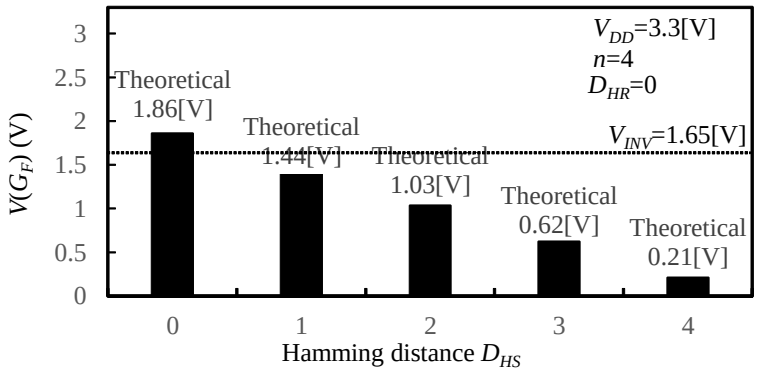
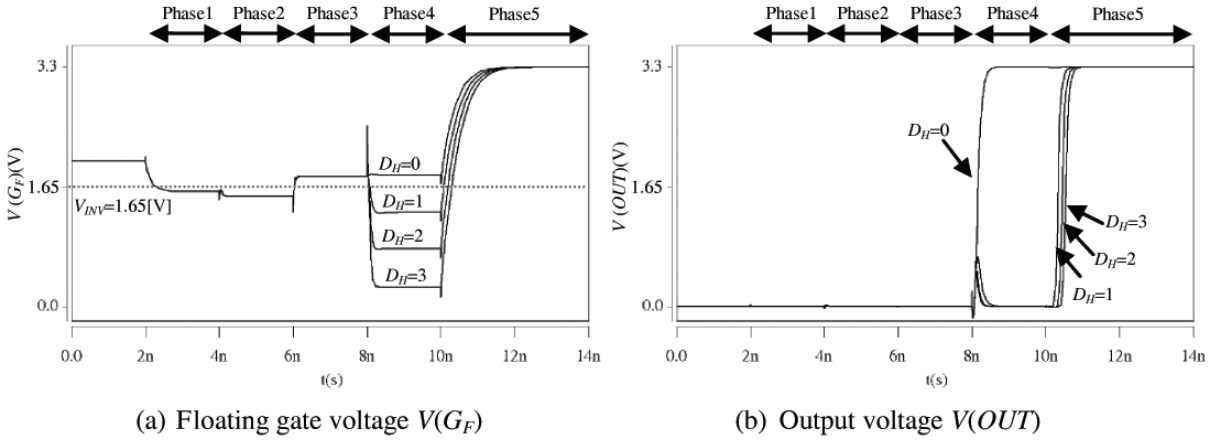


FIGURE 3. The floating gate voltage of the clocked neuron CMOS inverter in Phase 4

TABLE 2. Device parameters and simulation conditions

Symbol	Value	Units
V_{DD}	3.3	V
n	4	–
R	1	kΩ
W_n/L_n	5/2	μm
W_p/L_p	15/2	μm
C	16	fF

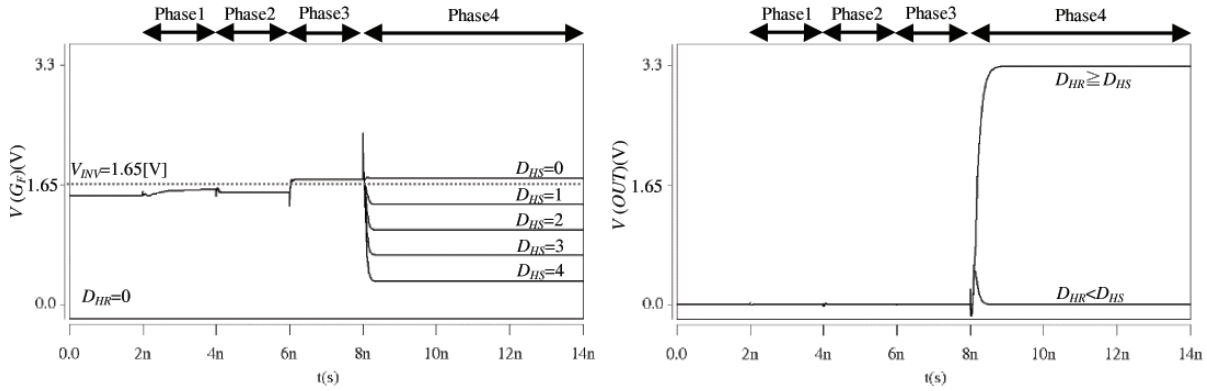


(a) Floating gate voltage $V(G_F)$ (b) Output voltage $V(OUT)$

FIGURE 4. Simulation results of the conventional circuit

using the voltage domain shown in Figure 3. On the other hand, in the conventional circuit, the Hamming distance is searched using the time domain. Therefore, the proposed circuit can search faster than the conventional circuit. Also, in the conventional circuit, when the next search operation is performed, calibration operation must be performed again from Phase 1, because the capacitors are charged from the current mirror. However, the proposed circuit can search continuously although this circuit must perform calibration at a certain interval for refreshing of the capacitors.

4. **Simulation Results.** These simulations were carried out using the ROHM Semiconductor 0.18μm CMOS process. Table 2 shows device parameters and simulation conditions. The floating gate voltage of the conventional circuit and the output $V(OUT)$ are shown in Figures 4(a) and 4(b). As shown in these figures, the conventional circuit searches for the Hamming distance with time difference.



(a) Floating gate voltage $V(G_F)$ (b) Output voltage $V(OUT)$

FIGURE 5. Simulation results of the proposed circuit

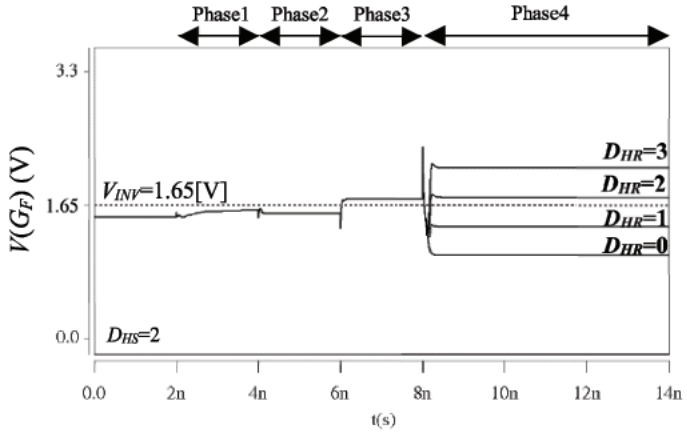


FIGURE 6. Simulation results of the floating gate voltage when the D_{HS} is 2

Figures 5(a) and 5(b) show the floating gate voltage of the proposed circuit and the output $V(OUT)$ when the reference distance D_{HR} is 0. The proposed circuit searches for the Hamming distance based on the magnitude relationship between the reference distance D_{HR} and the Hamming distance D_{HS}. When the Hamming distance D_{HS} is larger than the reference distance D_{HR}, the output voltage becomes 0[V]. On the other hand, when the Hamming distance D_{HS} is equal to or less than the reference distance D_{HR}, the output voltage becomes V_{DD}. As we can see from these figures, the proposed circuit performs the search operation using the voltage domain. In addition, since the searching process of the proposed circuit is not the time domain using the current mirror, it can be seen that the time required for the search is reduced. Moreover, Figure 6 shows the simulation result when the D_{HS} is 2. It can be seen that the reference distance setting signal of the proposed circuit can be operated theoretically.

5. **Conclusion.** This paper proposed a Hamming distance search circuit in voltage domain using clocked neuron CMOS inverter. Compared with the conventional circuit, the proposed circuit can realize a high-speed search by using the voltage domain. Also, due to the characteristics of this circuit, reduction of the number of times of calibration is conceivable. Furthermore, the number of the calibration operation can decrease by the characteristics of the proposed circuit.

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