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EXPERIMENT OF A HIGH VOLTAGE GAIN SWITCHED CAPACITOR DC-DC CONVERTER BASED ON A CROSS-CONNECTED FIBONACCI-TYPE CONVERTER

Ratanaubol Rubpongse[1], Farzin Asadi[2], Wanglok Do[1] and Kei Eguchi[1]

[1]Department of Information Electronics
Fukuoka Institute of Technology
3-30-1 Wajiro-higashi, Higashi-ku, Fukuoka 811-0295, Japan
mam17202@bane.fit.ac.jp; eguti@fit.ac.jp

[2]Department of Mechatronics Engineering
Kocaeli University
Umuttepe Yerleşkesi 41380, Kocaeli, Turkey
farzinsd@gmail.com

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Abstract. *To make an efficient converter for energy harvesting systems, a high voltage gain cross-connected switched-capacitor (SC) DC-DC converter is presented in this paper. By using a cross-connected structure based on Fibonacci-type converters, the proposed converter can realize high voltage gain, where the voltage gain is expressed as a power of two. On the other hand, unlike traditional converters, stepped-up voltage is created in every clock cycle. By using the cross-connected structure, the proposed converter can reduce the size of output capacitor and output ripple noise. Therefore, the proposed converter can be compact in size. Experimentation revealed that the proposed converter can realize a high voltage gain, fast response speed, small output ripple noise, even at a small size.*

Keywords: Charge pump, Cross-connected topology, Energy harvesting system, Fibonacci converters

1. **Introduction.** In the future, the earth will face problems with energy shortages and environmental pollution. To solve these problems, the technology of clean energy harvesting systems undergoes continuous development for the various sources of clean energy, such as thermoelectricity, light, and vibration. Those clean energy harvesting systems must be combined with converters. These clean energy sources are normally small. As a result, the power converter must be small in size with high voltage gain in order to develop efficient energy harvesting systems. To reduce circuit size, many converter circuits have to be designed as inductorless switched-capacitors for changing to an integrated circuit because it can achieve no flux of magnetic induction. However, the traditional converter has to connect with a large output capacitor. It is known that the occupational integrated circuit area of a capacitor is large.

For many decades, there are many researchers who have developed switched-capacitor converters. For example, Wang et al. developed a reconfigurable switch-capacitor DC-DC converter for energy harvesting system [1] and Yun et al. researched about a charge pump circuit using multivibrator for thermoelectric generator [2,3]. However, the voltage gain of both converters is proportional to the number of stages such as $(N + 1)\times$ $(N = 1, 2, 3, \ldots)$. Consequences of the voltage gain equation, these converters should be designed by connecting many stages to make high voltage gain. Moreover, these converters create a stepped-up voltage in a half clock cycle. The output capacitor should be large to minimize

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ripple noise. From two reasons above, the occupation area of these converters is very large when becoming a chip.

Following these studies, Eguchi et al. proposed a step-up/step-down $k(= 2, 3, \ldots)$-Fibonacci DC-DC converter [4]. The $k(= 2, 3, \ldots)$-Fibonacci converter can actualize high voltage gain. However, a large output capacitor is essential to reduce output ripple, because the Fibonacci converter generates a stepped-up voltage only in a half clock cycle. Furthermore, the large output capacitor makes the response speed to be slow. Eguchi et al. suggested a cross-connected charge pump, where the voltage gain is expressed as $2N \times V_{in}$ $(N = 1, 2, 3, \ldots)$ [5]. By using a cross-connected structure, a cross-connected charge pump can reduce the size of the output capacitor, because the stepped-up voltage is created in every clock cycle. However, the circuit size will become large if the input voltage is small, because the voltage gain of the cross-connected charge pump is still small.

This paper proposes a high voltage DC-DC converter for developing efficient energy harvesting systems. By the cross-connected structure based on Fibonacci-type converters, the proposed converter can accomplish high voltage gain, such as $2^N \times V_{in}$ $(N = 1, 2, 3, \ldots)$, and reduce ripple output noise. Conversely, unlike traditional converters, a big output capacitor is not necessary. Consequently, the proposed converter is appropriate to energy harvesting systems. To explore the circuit's characteristics and its efficiency, experiments were carried out concerning the experimental circuit constructed with commercially available components on a breadboard.

The structure of this paper is as follows. In Section 2, the circuit configuration and equation of voltage gain of the proposed converter and the Fibonacci converter are illustrated. Section 3 shows a comparison of circuit components between the proposed converter and the Fibonacci converter. Section 4 shows the experimental results of the proposed converter and the Fibonacci converter. Lastly, Section 5 summarizes the results of this study and future works.

2. **Circuit Configuration.**

2.1. **Traditional converter.** Figure 1 shows the circuit configuration of the Fibonacci converter in the transformation ratio of 8 by driving transistor switches S1 and S2 controlled by non-overlap two phase clock pulses. The output voltage of the proposed converter is expressed by

$$V_{N+2} = V_N + V_{N+1}, \quad (N \geq 0) \tag{1}$$

where the parameter N denotes the number of stages. By N $(= 0, 1, 2, 3, 4)$, the output voltage becomes V_{in}, $2V_{in}$, $3V_{in}$, $5V_{in}$, and $8V_{in}$. In the case of Figure 1, the parameter N is 4. Equation (1) shows the voltage gain of the Fibonacci converter. Furthermore, in Fibonacci converters, stepped-up voltage is created in only half clock cycles. Therefore, the Fibonacci converter requires a large output capacitor C_{out} to reduce ripple output.

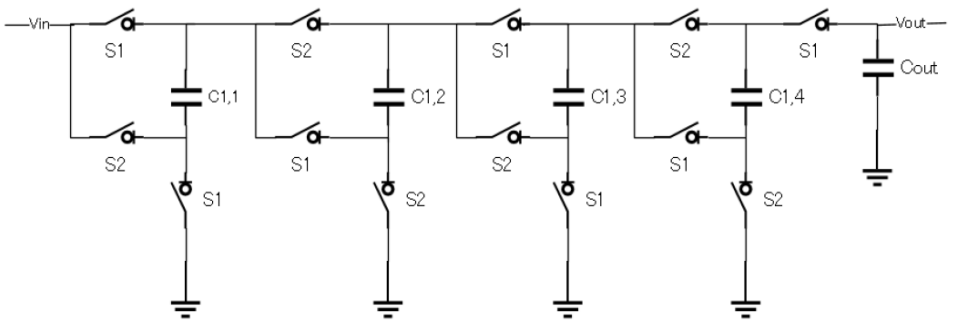


FIGURE 1. Circuit configuration of the Fibonacci converter in the transformation ratio of 8

In the conversion ratio of 8, the Fibonacci converter characteristic of voltage gain is analyzed theoretically to find the equation of relationship between input voltage V_{in}, output voltage V_{out}, and the voltage of the main capacitors as (2) and (3).

When switch S1 is on the values of input voltage and output voltage when the internal resister is 0, V_{in} and V_{out} are expressed as

$$\begin{aligned} V_{c_{1,1}} &= V_{in} \\ V_{c_{1,3}} &= V_{c_{1,2}} + V_{in} = 2V_{in} + V_{in} = 3V_{in} \\ V_{out} &= V_{c_{1,4}} + V_{c_{1,3}} = 5V_{in} + 3V_{in} \\ V_{out} &= 8V_{in} \end{aligned} \tag{2}$$

When switch S2 is on and the internal resister is 0, the voltages of the main capacitors are expressed as

$$\begin{aligned} V_{c_{1,2}} &= V_{c_{1,1}} + V_{in} = 2V_{in} \\ V_{c_{1,4}} &= V_{c_{1,3}} + V_{c_{1,2}} = 3V_{in} + 2V_{in} = 5V_{in} \end{aligned} \tag{3}$$

2.2. **Proposed converter.** Figure 2 shows the circuit configuration of the proposed converter in the transformation ratio of 8, by driving transistor switches S1 and S2 controlled by non-overlap two phase clock pulses. The output voltage of the proposed converter is expressed by

$$V_{out} = 2^N \times V_{in}, \quad (N > 0) \tag{4}$$

where the parameter N denotes the number of stages. In the case of Figure 2, the parameter N is 3. As (4) shows, the proposed converter can achieve to make ultra-high voltage gain easier than traditional converters. Moreover, the stepped-up voltage is created in all clock cycles. Therefore, the proposed converter does not require a large output capacitor. Furthermore, by using a cross-connected structure, it is possible to reduce circuit size and improve response speed.

In the conversion ratio of 8, the proposed converter characteristic of voltage gain is analyzed theoretically to find an equation of the relationship between input voltage V_{in} and output voltage V_{out} as (5) and (6).

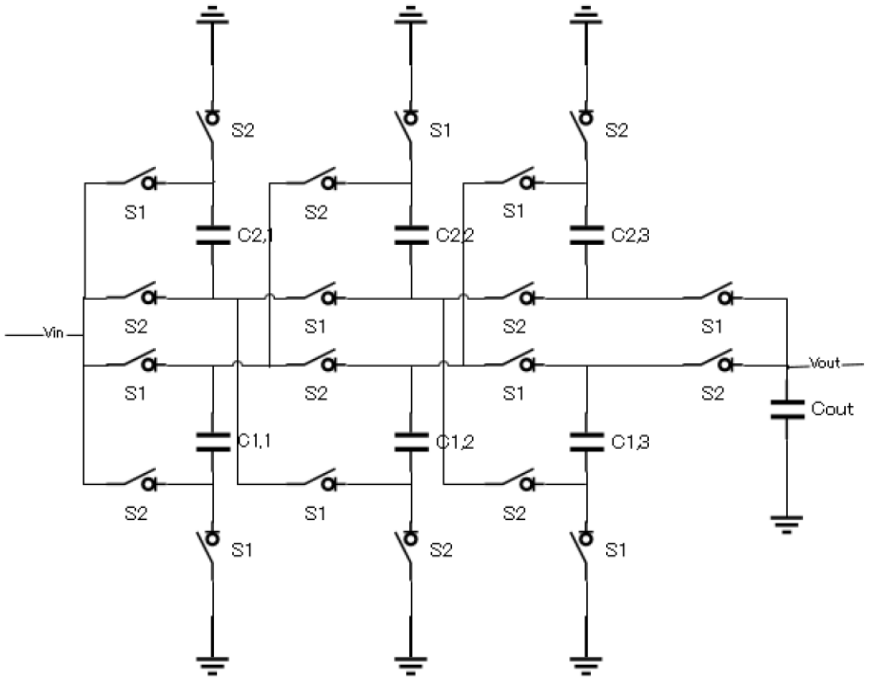


FIGURE 2. Circuit configuration of the proposed converter in the transformation ratio of 8

When switch S1 is on the values of input voltage and output voltage when the internal resister is 0, V_{in} and V_{out} are expressed as

$$\begin{aligned} V_{c_{1,1}} &= V_{in} \\ V_{c_{2,2}} &= V_{c_{2,1}} + V_{in} = 2V_{in} \\ V_{c_{1,3}} &= V_{c_{1,2}} + V_{c_{2,1}} + V_{in} = 4V_{in} \\ V_{out} &= V_{c_{2,3}} + V_{c_{1,2}} + V_{c_{2,1}} + V_{in} \\ V_{out} &= 4V_{in} + 2V_{in} + V_{in} + V_{in} \\ V_{out} &= 8V_{in} \end{aligned} \tag{5}$$

When switch S2 is on the values of input voltage and output voltage when the internal resister is 0, V_{in} and V_{out} are expressed as

$$\begin{aligned} V_{c_{2,1}} &= V_{in} \\ V_{c_{1,2}} &= V_{c_{1,1}} + V_{in} = 2V_{in} \\ V_{c_{2,3}} &= V_{c_{2,2}} + V_{c_{1,1}} + V_{in} = 4V_{in} \\ V_{out} &= V_{c_{1,3}} + V_{c_{2,2}} + V_{c_{1,1}} + V_{in} \\ V_{out} &= 4V_{in} + 2V_{in} + V_{in} + V_{in} \\ V_{out} &= 8V_{in} \end{aligned} \tag{6}$$

3. **Comparison.** Table 1 presents the comparison of the number of circuit components of the Fibonacci converter and the proposed converter in the conversion ratio of 8. The number of switches and capacitors in the proposed converter is more than that in the Fibonacci converter.

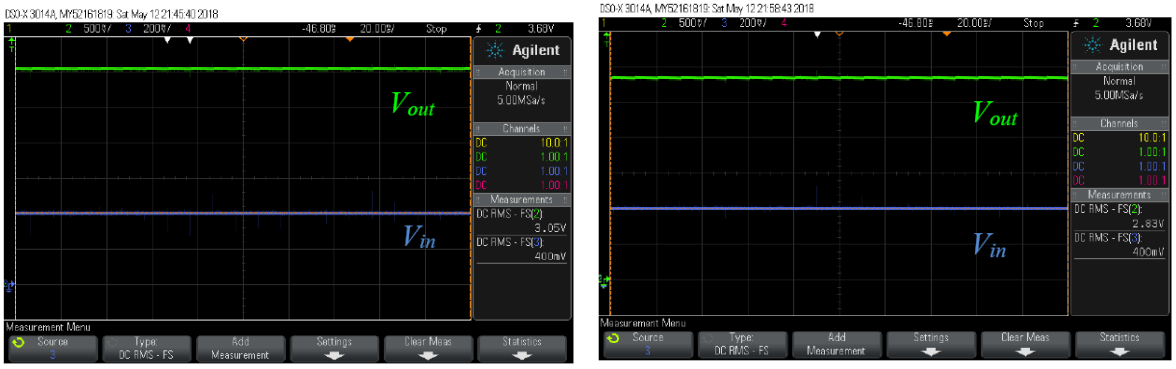
TABLE 1. Comparison of the number of circuit components

	Number of switches	Number of capacitors
Fibonacci converter in the conversion ratio of 8	13	5 (C_{out} = 22 μF, 4.7 μF)
Proposed converter in the conversion ratio of 8	20	7 (C_{out} = 22 μF, 4.7 μF)

However, the proposed converter stepped-up voltage can be created in every clock cycle. Thus, the proposed converter does not require a large output capacitor. Conversely, traditional converters' stepped-up voltage is created in only half clock phases. Thus, to reduce ripple noise, the large capacitor output is essential. On the other hand, when changed to become an integrated circuit, the size of capacitors switches is larger than the size of a transistor. As a result, the size of traditional converter circuit is larger than the size of the circuit of the proposed converter.

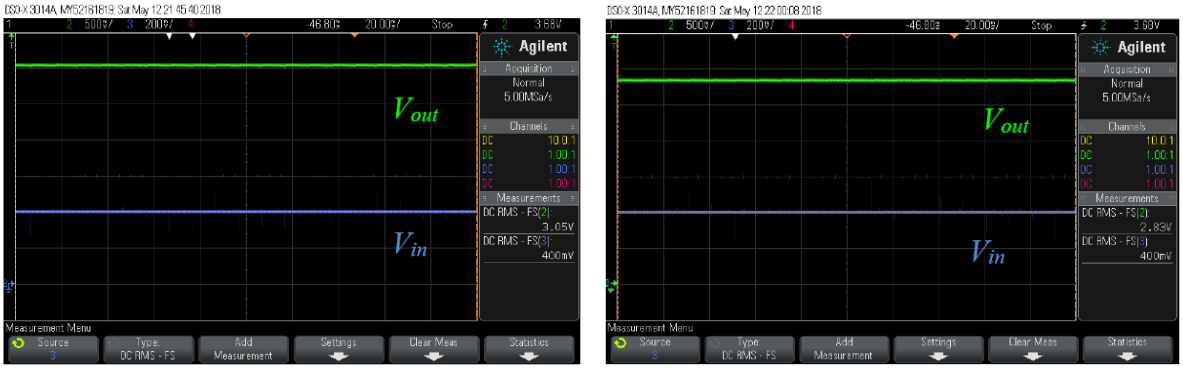
4. **Experimental Results.** The experiment was conducted under the following conditions: the input voltage V_{in} = 400 mV, the capacitance of the proposed converter and the Fibonacci converter $C_{1,1} = \cdots = C_{1,3}$ = 1 μF, C_{out} = 4.7 μF and 22 μF, the value of frequency f = 50 Hz, output load R_{load} = 68 kΩ – 2.2 MΩ.

The first experiment was checking voltage output of the proposed converter and the Fibonacci converter. For the proposed converter, when the output capacitor is 4.7 μF, 22 μF, by R_L = 2.2 MΩ, the output voltage is 3.05 V as shown in Figure 3(a) and Figure 4(a). By R_L = 470 kΩ, the output voltage is 2.83 V as Figure 3(b) and Figure 4(b) show. For the Fibonacci converter, when the output capacitor is 4.7 μF, 22 μF, by R_L = 2.2 MΩ, the output voltage is 2.96 V as Figure 5(a) and Figure 6(a) show. By R_L = 470 kΩ, the output voltage is 2.68 V as shown in Figure 5(b) and Figure 6(b). The experiment found that for the Fibonacci converter, when the output capacitor is small, the output voltage has a huge ripple noise as shown in Figure 5(a). Furthermore, the output voltage



(a) (b)

FIGURE 3. Input voltage and output voltage of the proposed converter from the oscilloscope when the output capacitor is 4.7 μF. (a) $R_L = 2.2$ MΩ and (b) $R_L = 470$ kΩ.



(a) (b)

FIGURE 4. Input voltage and output voltage of the proposed converter from the oscilloscope when the output capacitor is 22 μF. (a) $R_L = 2.2$ MΩ and (b) $R_L = 470$ kΩ.

(a) (b)

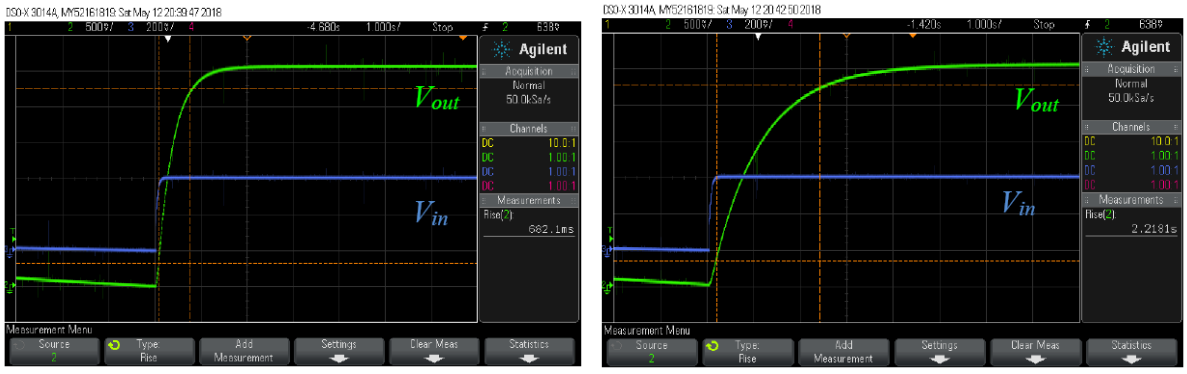
FIGURE 5. Input voltage and output voltage of the traditional converter when the output capacitor is 4.7 μF. (a) $R_L = 2.2$ MΩ and (b) $R_L = 470$ kΩ.

(a) (b)

FIGURE 6. Input voltage and output voltage of the traditional converter when the output capacitor is 22 μF. (a) $R_L = 2.2$ MΩ and (b) $R_L = 470$ kΩ.

of both converters depends on the output resistor; if the output resistor is very large, the output voltage is close to the theory value.

The second experiment showed the response speed between the proposed converter and the Fibonacci converter, where the output resister R_L was set to 2.2 MΩ. For the proposed converter, by $C_{out} = 4.7$ μF, the risk time is 682.1 msec as shown in Figure 7(a); by $C_{out} = 22$ μF, the risk time is 2.2181 sec as Figure 7(b) shows. For the Fibonacci converter, by $C_{out} = 4.7$ μF, the risk time is 960.3 msec as Figure 8(a) shows. By $C_{out} = 22$ μF, the risk time is 3.0622 sec as Figure 8(b) shows. Based on the experiment, the response speed of both converters depends on output capacitor C_{out}. However, the response speed of the proposed converter is faster than the Fibonacci converter by the same capacitor value.



(a) (b)

FIGURE 7. Output and input voltage as a function of time of the proposed converter. (a) The output capacitor is 4.7 μF and (b) the output capacitor is 22 μF.

The third experiment is a comparison of voltage gain between the proposed converter and the Fibonacci converter. When R_{load} is between 330 Ω to 680 kΩ, the result is as shown in Figure 9. The voltage gain of both converters depends on the output power. If the output power is low, the voltage gain is close to the ideal value 8×. However, the voltage gain of the proposed converter is higher than the traditional converter with the same output power.

(a) (b)

FIGURE 8. Output and input voltage as a function of time of the traditional converter. (a) The output capacitor is 4.7 μF and (b) the output capacitor is 22 μF.

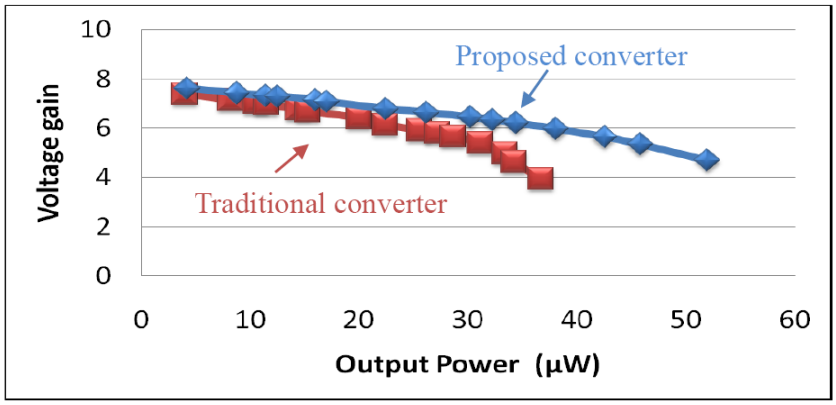


FIGURE 9. Voltage gain as a function of output power

5. **Conclusions.** To solve problems with energy shortages and environmental pollution, with energy harvesting systems, a cross-connected switched-capacitor (SC) DC-DC converter has been proposed in this paper. The results of theoretical and experimental data substantiated the following results. 1) By using a cross-connected structure based on Fibonacci-type converters, the proposed converter can realize high voltage gain and small ripple noise. 2) The proposed converter can be compact in size because it does not require a large output capacitor and the size of the proposed converter will be smaller than the traditional converter. 3) When the output capacitor size of the traditional converter is not enough, it causes a problem of ripple noise. To reduce ripple noise, the traditional converter does require a large output capacitor. However, the size of the circuits depends on the output capacitor, and the output capacitor will make the circuit size large in scale and make the response speed slow. 4) The response speed of the proposed converter is faster than the traditional converter under the same conditions.

In a future study, we are going to experiment to find the power efficiency and experiment with the conditions of the same integrated circuit for the design of high efficiency converter chips.

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