ICIC Express Letters
Volume **14**, Number **1**, January **2020**

ICIC International ©2020 ISSN 1881-803X
pp. 81–87

COMPARISON OF DIFFERENT TECHNIQUES TO IDENTIFY THE BEST LOCATION OF SVC TO ENHANCE THE VOLTAGE PROFILE

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Received May 2019; accepted August 2019

Abstract. *Nowadays power system has become a more complex network due to ever increasing electricity demand and the open access electricity market activities. FACTS devices play an imperative role for enhancing the steady state and dynamic performance of the power system. Static VAR compensators (SVCs) have capability of controlling the reactive power flow. These shunt FACTS devices are considered in this paper for enhancement of voltage profile of the system. In this paper, a comparative analysis of three different techniques (namely FVSI, LSF and RPL) has been exhibited to identify the location of SVCs in order to achieve the objective of voltage profile enhancement. In this paper five loading conditions are also considered for evaluating the effectiveness and robustness of aforesaid techniques.*

Keywords: Voltage profile, Fast voltage stability index, Line stability factor, Reactive power loading, Static VAR compensator (SVC), Voltage stability margin (VSM)

1. **Introduction.** Today's power system is quite a vast and complex interconnected system, so it becomes essential to operate the power system in an efficient and secure manner. Continuously changing load pattern and ever increasing power demand adversely affect the power flow in transmission line. The voltage of power system gets collapsed because of unequal load distribution which poses a threat to the power system security. Under high stressed conditions voltage may fall gradually or it may also even collapse. FACTS controllers are found to be an effective alternative for improving the steady state and dynamic voltage performance of the system [1-3]. FACTS devices are capable of changing the power, phase angle, voltage at particular points in power system. FACTS device also works as fast control actions controller, self commutated power electronics converters for ensuring security of power system [4-6]. FACTS devices are required to be installed at appropriate locations in order to avail maximum benefits. The types of the FACTS devices are decided according to the need of individual application. It is preferable to select shunt controllers where the voltage support is required and series controllers incorporated where line flow control is required [7,8]. The SVC is most frequently used among shunt FACTS devices due to its low cost and good performance in system enhancement [9-11]. It can flexibly control the generation as well as absorption of reactive power at the point where it is connected. These devices provide a better transformation to various operational conditions and enhance the usage of existing installations. The effectiveness of FACTS devices mainly depends on the location of its control devices. The optimum location of FACTS devices is very essential in power system since the weakest bus is required to be identified [12,13]. Many techniques are proposed for allocating FACTS devices at their optimal location for stability analysis. Some of proposed methods in literature are

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DOI: 10.24507/icicel.14.01.81

P-V and Q-V curve based indices, Jacobin matrix singularity indices, power flow solution pairs and L-index. It is quite evident to commit that FACTS device are incorporated for controlling reactive power and also used for enhancing voltage stability [14-16].

Nowadays, various techniques have been suggested and applied by various researchers to obtain the best location and parameter settings of FACTS devices to enhance power system performance in terms of congestion management, improvement in reliability, stability, and security. However, different techniques may determine various locations for placement of SVC.

Hence, this work is inspired from facing the difficulties in identifying the most efficient technique for determining the most suitable location of SVC.

In this paper, comparative analysis of FVSI, LSF and RPL techniques is presented to determine suitable location of SVC for improving voltage profile of the system. The effectiveness of the aforesaid techniques is tested on IEEE 9 bus system with different loading conditions.

Section 1 presents state of art literature on shunt FACTS devices such as static VAR compensator which are used for enhancement of voltage profile. The fundamental concepts of different techniques are described in Section 2. The algorithms of different techniques are explained in Section 3. The results are briefly demonstrated and discussed in Section 4. Finally, Section 5 gives the concluding remark.

2. Different Methodologies for Identification of Critical Bus for SVC Placement.

Various methodologies have been proposed in the literature for the placement of shunt FACTS devices. Out of them, three latest techniques have been considered in this paper for determining the suitable locations of SVCs. The detailed analysis along with algorithm of each is explained in below sub sections.

2.1. Fast voltage stability index technique.

The FVSI is based on the concept of power flow through a single line [17]. It has been formulated as:

$$FVSI = \frac{4Z^2 \cdot Q_r}{V_s^2 \cdot X} \tag{1}$$

where Z – line impedance; Q_r – reactive power at receiving bus; X – line reactance; V_s – voltage of the sending bus.

If its value is close to 1 it indicates the particular line is closed to its instability point and it may lead to voltage collapse in the entire system.

2.2. Line stability factor.

The line stability factor can be calculated from the equation below as [18]:

$$LSF = 4\left(\frac{X}{V_i^2}\right)\left(\frac{X}{V_i^2}P_i^2 + Q_j\right) \tag{2}$$

where X – reactance of the line; Q_j – reactive power at the receiving bus; V_i – voltage at the sending bus; P_i – active power at the sending bus.

To maintain a safe condition, LSF factor should be maintained below 1.

2.3. Reactive power loading.

Reactive power loading technique is based on a general concept, which states that with an increase in reactive power loading of different buses of the system, the voltage profile will alter. After a certain point with increasing reactive power load the power flow program will not converge. This certain point is known as maximum loading point. The voltage at maximum loading point is known as critical voltage. The VSM (voltage stability margin) of each bus is calculated by the following formula [19]:

$$VSM = \frac{V_b(base\ value) - V_c(critical\ value)}{V_c(critical\ value)} \tag{3}$$

where, V_b – base value of bus voltage; V_c – critical value of bus voltage.

For secure condition, the value of VSM (voltage stability margin) is always less than 1.

3. Algorithms.

A. The algorithm for SVC's placement using FVSI and LSF techniques is as follows:

Step-1: Data of IEEE9 bus system is collected, studied and the system is simulated using PSCAD simulation software.
Step-2: Assign the next load bus for reactive power loading.
Step-3: Increased the reactive power load of certain load bus is increased to 150% of their base value and perform the power flow analysis.
Step-4: Compute the FVSI and LSF for each bus of the network system.
Step-5: Check the stop criteria (FVSI ≥ 1) and (LSF ≥ 1); if criteria are satisfied then go to step 6; else go to step 2.
Step-6: Select the highest ranking of bus for device placement of fact device.

B. The algorithm of RPL technique is as follows:

Step-1: Data of IEEE 9 bus system is collected, studied and the system is simulated using PSCAD simulation software.
Step-2: Reactive power of all load buses is increased step by step, till the maximum reactive loading point is achieved.
Step-3: At 150% reactive loading condition the maximum reactive power loading point achieve, the power flow program will not converge.
Step-4: Calculate the voltage stability margin (VSM) for each bus of the network system.
Step-5: The bus having highest value of voltage stability margin (VSM) is selected as most critical bus of the network system.

4. Results and Discussion.

The single line diagram of IEEE 9 bus system is shown in Figure 1 and the simulation diagram of IEEE 9 bus system in PSCAD software is also shown in Figure 2. The data of IEEE 9 bus system is given in [20]. Bus 1 is considered as the slack bus.

To test the effectiveness of the above mentioned approaches, IEEE 9 bus system is simulated in PSCAD software. Three different cases are considered for comparative analysis

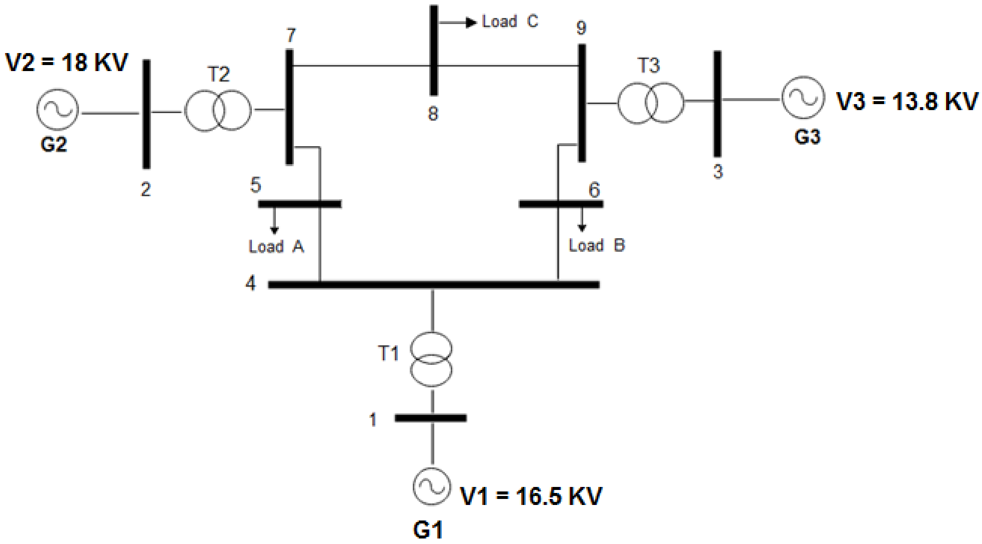

Figure 1. Single line diagram of IEEE 9 bus system

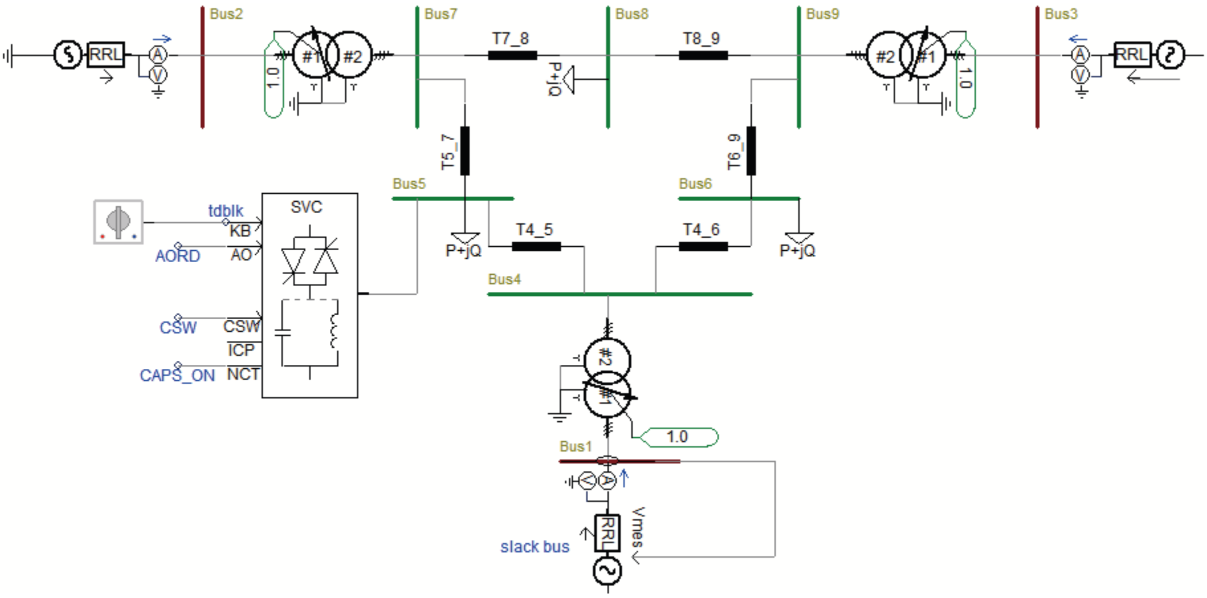

Figure 2. IEEE 9 bus system in PSCAD simulation software

of different techniques for enhancement of voltage stability. The static VAR compensator (SVC) inserted in the system with following parameters:

Inductive MVAR = 100 MVAR
Rating of Transformer = 200 MVA
Rating of SVC = 150 MVAR
Rated Frequency of SVC= 60 Hz

4.1. **Case I (without SVC placement).** In this case, base load condition of IEEE 9 bus system is considered. Table 1 exhibits the value of loads ($P\&Q$) at different load levels. The voltages of different buses (without SVC installation) at five different loading conditions are shown in Table 2.

Table 1. Values of $P\&Q$ at different loading conditions

Loading %	Loading on 5th bus		Loading on 6th bus		Loading on 8th bus	
	P (MW)	Q (MVAR)	P (MW)	Q (MVAR)	P (MW)	Q (MVAR)
100	125.0	50.0	90.0	30.0	100.0	35.00
105	131.25	52.5	94.5	31.5	105.0	36.75
110	137.50	55.00	99.0	33.0	110.0	38.75
115	143.75	57.50	103.5	34.5	115.0	40.23
120	150.0	60.0	108.0	36.0	120.0	42.00
125	156.25	62.50	112.5	37.50	125.0	43.75

Table 2. Voltage of each bus at different loading conditions without SVC

Loading %	Voltage of each bus without SVC in (p.u.)								
	1	2	3	4	5	6	7	8	9
100	1.00	0.99	0.99	0.98	0.95	0.97	0.99	0.98	0.99
105	1.00	0.98	0.97	0.97	0.94	0.96	0.97	0.96	0.98
110	1.00	0.96	0.96	0.97	0.93	0.94	0.96	0.94	0.96
115	1.00	0.94	0.94	0.96	0.92	0.93	0.94	0.92	0.95
120	1.00	0.92	0.92	0.94	0.90	0.91	0.92	0.90	0.92
125	1.00	0.89	0.88	0.92	0.86	0.89	0.88	0.86	0.89

4.2. **Case II (SVC placement using FVSI & LSF techniques).** In this case the fast voltage stability and line stability factor techniques are considered for identifying the critical bus for SVC placement. The FVSI and line stability factor techniques are executed on different load buses with 150% reactive loading condition. Results for case II are illustrated in Tables 3 and 4 respectively.

Table 3. FVSI values for different load buses at 150% reactive loading condition

Load	5th bus	6th bus	8th bus
$Q = 172.5$ (MVAR)	0.1198	0.8625	0.0925

Table 4. LSF values for different load buses at 150% reactive loading condition

Load	5th bus	6th bus	8th bus
$Q = 172.5$ (MVAR)	0.1701	0.1517	0.0726

Tables 3 and 4 show the critical bus is identified at bus no. 5 for the placement of SVC by FVSI & LSF techniques respectively.

Table 5 demonstrates the per unit voltage of each bus of the system with five different loading conditions after placing the SVC at bus no. 5. The voltage of bus no. 5 is effectively improved from 0.86 p.u. to 0.96 p.u. at 125% loading condition.

Table 5. Voltage of each bus at different loading conditions with SVC (at bus no. 5)

Loading %	Voltage of each bus with SVC in (p.u.)								
	1	2	3	4	5	6	7	8	9
100	1.00	1.01	1.01	1.00	0.99	0.99	1.01	1.00	1.01
105	1.00	1.00	1.00	1.00	0.99	0.98	1.00	0.99	1.00
110	1.00	0.99	0.99	1.00	0.99	0.97	1.00	0.98	0.99
115	1.00	0.98	0.97	0.99	0.99	0.97	0.99	0.97	0.98
120	1.00	0.96	0.96	0.99	0.98	0.96	0.97	0.95	0.97
125	1.00	0.94	0.93	0.97	0.96	0.94	0.94	0.92	0.94

4.3. **Case III (SVC placement using RPL technique).** In this case the reactor power loading technique is considered for identification of critical bus for SVC placement. The RPL technique is executed on different load buses with 150% reactive loading condition. Results for case III are illustrated in Table 6.

Table 6. RPL values of different buses at 150% loading condition

Load	5th bus	6th bus	8th bus
$Q = 172.5$ (MVAR)	0.1012	0.11632	0.13569

Table 6 revealed that critical bus is identified at bus no. 8 for the placement of SVC by RPL technique.

Table 7 depicted that the voltage of bus no. 8 is improved from 0.86 p.u. to 0.99 p.u. at 125% loading condition.

Table 8 compared the minimum voltage of each bus under various loading conditions, with SVC device obtained using FVSI, LSF and RPL techniques.

Table 7. Voltage of each bus at different loading conditions with SVC (at bus no. 8)

Loading %	Voltage of each bus with SVC in (p.u.)								
	1	2	3	4	5	6	7	8	9
100	1.00	1.00	1.00	0.98	0.96	0.98	1.00	1.00	1.01
105	1.00	1.00	1.00	0.98	0.96	0.97	1.00	0.99	1.00
110	1.00	0.99	0.99	0.98	0.95	0.97	1.00	0.99	1.00
115	1.00	0.99	0.99	0.98	0.95	0.96	0.99	0.99	1.00
120	1.00	0.98	0.98	0.97	0.94	0.96	0.99	0.99	0.99
125	1.00	0.98	0.98	0.97	0.94	0.95	0.99	0.99	0.99

Table 8. Comparison of voltage profile of each bus with different loading conditions at different weak bus locations of SVC

Loading %	(FVSI & LSF techniques) SVC place at bus no. 5		(RPL technique) SVC place at bus no. 8	
	Minimum bus voltage (p.u.)	Bus number	Minimum bus voltage (p.u.)	Bus number
100	0.99	6	0.96	5
105	0.98	6	0.96	5
110	0.97	6	0.95	5
115	0.97	6	0.95	5
120	0.95	8	0.94	5
125	0.92	8	0.94	5

5. **Conclusion.** The power systems across the world are being operated at highly loaded conditions, as a result of which they are becoming more prone to voltage instability. In order to overcome this problem of voltage instability, it is necessary to determine the optimal location of voltage compensating device like SVC. Mainly, there are three techniques to solve the SVC's allocation problem namely as FVSI, LSF and RPL. In this paper, the comparative analysis of all three techniques has been presented. The standard IEEE 9 bus system has been considered as test bus system. The comparative results show that FVSI and LSF methods are better than RPL technique. The FVSI & LSF techniques give better location for SVC installation than RPL technique. The aforesaid techniques can be applied and tested for dynamic load also in future research work.

Acknowledgments. The authors like to acknowledge the Swami Keshvanand Institute of Technology Management & Gramathon (SKITM&G), Jaipur and Department of Electrical Engineering for their support and encouragement.

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