ICIC Express Letters
Volume **14**, Number **10**, October **2020**

 ISSN 1881-803X
pp. **985–992**

ANALYSIS BY FPD FOR NEURON CMOS VARIABLE LOGIC CIRCUIT WITH FG CALIBRATION

Riku Ohtsuka[1], Hayato Yagi[1], Masaaki Fukuhara[1] and Kuniaki Fujimoto[2]

[1]Department of Embedded Technology
School of Information and Telecommunication Engineering
Tokai University
2-3-23, Takanawa, Minato, Tokyo 108-8619, Japan
9bjnm004@mail.u-tokai.ac.jp; fukuhara@tokai.ac.jp

[2]School of Industrial and Welfare Engineering
Tokai University
9-1-1, Toroku, Higashi, Kumamoto 862-8652, Japan
fujimoto@tokai.ac.jp

Received March 2020; accepted June 2020

Abstract. *A neuron CMOS variable logic circuit is used as a logic element of FPGA. Since the basic neuron CMOS variable logic circuit has a floating gate (FG) which is disconnected nowhere in the circuit, the basic circuit has a possibility to cause a malfunction due to the influence of the initial charge accumulated in the FG. Although the neuron CMOS variable logic circuit with FG calibration was proposed to solve the problem, the operation of the proposed circuit has not been analyzed. In this paper, we analyze the proposed neuron CMOS variable logic circuit with FG calibration by using FPD (Floating-Gate Potential Diagram) and perform the HSPICE simulation. These results are shown that the operation of the proposed circuit is proper.*
Keywords: FPGA, Variable logic circuit, Neuron CMOS inverter, FPD

1. **Introduction.** With the progress of integrated circuits in recent years, an increase in circuit scale has become a problem. As a method to solve this problem, FPGA which can dynamically change the circuit configuration by external signals is attracting attention. FPGA is called field programmable gate array because FPGA (Field Programmable Gate Array) allows users to change the circuit at hand. In order to realize the logic circuit element of FPGA, a single output variable logic circuit (**ν**CMOS variable logic circuit) using a neuron CMOS inverter (**ν**CMOS) was proposed [1,2]. However, **ν**CMOS can cause malfunction due to chip manufacturing. Although the neuron CMOS variable logic circuit with FG calibration has been proposed to solve the problem, the circuit has not been substantiated for variable logic operation [3]. In this paper, we analyze the circuit by clearly showing the output voltage corresponding to the input voltage using FPD (Floating-Gate Potential Diagram) [4]. Furthermore, we verify the behavior of the circuit's HSPICE simulation results matches the behavior analyzed by the FPD. As a result, we verify the circuit is operating normally.

2. **The Basic Variable Logic Circuit.** Figure 1 shows the configuration of the basic **ν**CMOS variable logic circuit [1]. This circuit has a configuration in which four-input and five-input **ν**CMOS (**ν**$\mathrm{CMOS_P}$ and **ν**$\mathrm{CMOS_M}$) are cascaded via a CMOS buffer circuit. V_{inA} and V_{inB} are input signals in the logic function. The buffer circuit is to amplify the voltage of V_m to V_{DD} or *GND*. Furthermore, the output voltage V_{OUT} of **ν**$\mathrm{CMOS_M}$ is

DOI: 10.24507/icicel.14.10.985

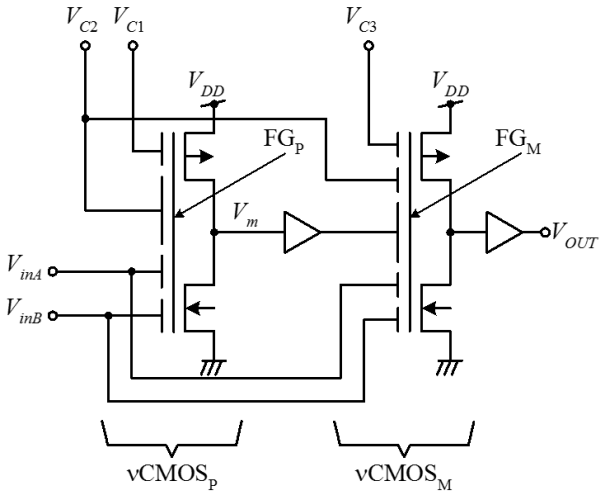

FIGURE 1. Basic neuron CMOS variable logic circuit

outputted through the other buffer. By setting three control signals (V_{C1}, V_{C2}, V_{C3}), logic functions are defined, and eight logic functions can be expressed.

However, the floating gates FG_P of νCMOS$_P$ and FG_M of νCMOS$_M$ are not connected anywhere in the circuit. Therefore, there is a possibility of malfunction due to the influence of initial charge at the time of chip manufacturing.

3. **νCMOS Variable Logic Circuit with FG Calibration.** In Figure 2, the proposed circuit is configured cascade two 5-input νCMOSs (νCMOS$_P$ and νCMOS$_M$) with different capacity ratios.

G_{P1}-G_{P5} and G_{M1}-G_{M5} are the input gates in νCMOSs, respectively. FG_P and FG_M are floating gates in νCMOSs, respectively. C_{P1}-C_{P5} and C_{M1}-C_{M5} are the input gate

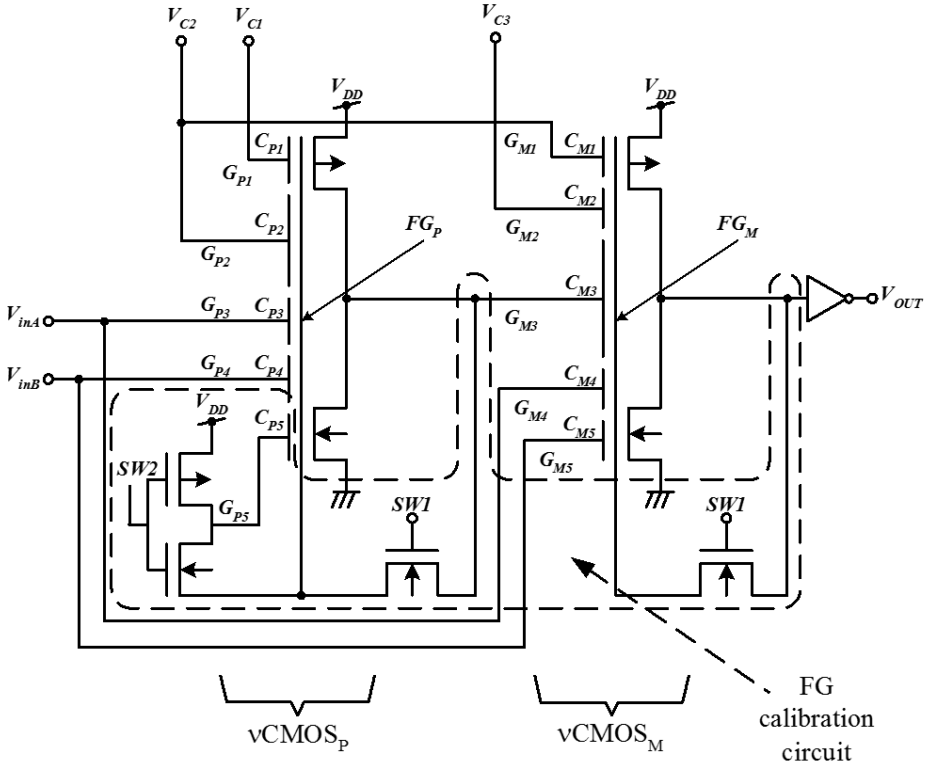

FIGURE 2. νCMOS variable logic circuit with FG calibration

capacitances in νCMOSs, respectively. Their capacity ratio is designed with $C_{P1} : C_{P2} : C_{P3} : C_{P4} : C_{P5} = 1 : 2 : 1 : 1 : 1$, $C_{M1} : C_{M2} : C_{M3} : C_{M4} : C_{M5} = 1 : 1 : 3 : 1 : 1$. V_{inA} and V_{inB} are input signals ("0" or "1"), V_{C1}, V_{C2}, and V_{C3} are control signals ("0" or "1") for switching logic functions, where "0" means 0 [V] and "1" means power supply voltage V_{DD}. Control signals SW_1 and SW_2 are for performing an FG calibration operation.

Next, in Figure 3, the FG calibration operation will be illustrated. The FG calibration operation is divided into PHASE1 and PHASE2. At this time, the input signals V_{inA} and V_{inB}, the control signals V_{C1}, V_{C2}, and V_{C3} always provide the logic signals shown in Table 1 through PHASE1 and PHASE2.

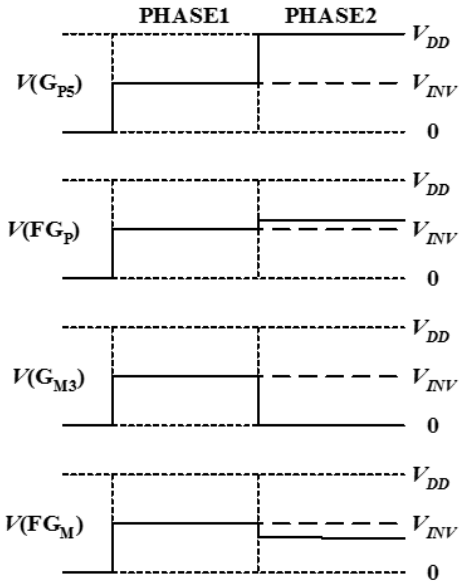

FIGURE 3. FG calibration operation

TABLE 1. Logic function table

FG calibration operation				
Control signal			Input	
V_{C1}	V_{C2}	V_{C3}	V_{inA}	V_{inB}
1	1	1	0	0

→

Variable logic operation			
Control signal			Logic function
V_{C1}	V_{C2}	V_{C3}	
0	0	0	OR
0	0	1	All-1
0	1	0	NOR
0	1	1	XNOR
1	0	0	XOR
1	0	1	NAND
1	1	0	All-0
1	1	1	AND

In PHASE1, SW_1 and SW_2 are changed to V_{DD}. Then, the output terminal in νCMOS$_P$, FG_P and G_{P5} are shorted. The voltage $V(FG_P)$ of FG_P and the voltage $V(G_{P5})$ of G_{P5} become Equation (1) regardless of the initial charge of FG_P.

$$V(FG_P) = V(G_{P5}) = V_{INV} = \frac{V_{DD}}{2} \tag{1}$$

In PHASE2, SW_1 and SW_2 are changed to 0 [V]. Then, the output terminals in νCMOS$_P$ and FG_P are disconnected, and $V(G_{P5})$ rises from the state of Equation (1) to

V_{DD}. The amount of change $\Delta V(FG_P)$ of $V(FG_P)$ from PHASE1 to PHASE2 becomes Equation (2).

$$\Delta V(FG_P) = \frac{C_{P5}}{C_{TP}} \left(V_{DD} - \frac{V_{DD}}{2} \right) \tag{2}$$

where C_{TP} in Equation (2) is the total capacitance of FG_P. Assuming the floating gate-substrate capacitance is sufficiently small, C_{TP} becomes Equation (3) using the gate capacitance ratio in νCMOS$_{\mathrm{P}}$ and a unit capacitance C.

$$C_{TP} = 6C \tag{3}$$

Therefore, $V(FG_P)$ of PHASE2 is given by Equation (4) from Equation (1), Equation (2) and Equation (3).

$$V(FG_P) = V_{INV} + \frac{C}{6C} \cdot \frac{V_{DD}}{2} \tag{4}$$

where the inversion threshold voltage V_{INV} of νCMOSs is VDD/2.

Next, variable logic operation will be described. The input and control signals change from the FG calibration operation as shown in Table 1. $V(FG_P)$ is raised in case V_{inA} or V_{inB} changes from "0". Similarly, $V(FG_P)$ is down in case V_{C1} or V_{C2} changes from "1". $V(FG_P)$ becomes Equation (5).

$$V(FG_P) = V_{INV} + \frac{C}{6C} \left(\frac{V_{DD}}{2} - V_{C1} - 2V_{C2} + V_{inA} + V_{inB} \right) \tag{5}$$

Similarly for νCMOS$_{\mathrm{M}}$, the voltage $V(FG_M)$ of the floating gate FG_M in the main inverter νCMOS$_{\mathrm{M}}$ can also be determined. In PHASE1, the voltage $V(G_{M3})$ of G_{M3} is $V_{DD}/2$ during the FG calibration operation. In PHASE2, $V(G_{M3})$ changes to V_{DD}. Thereafter, the pre-inverter νCMOS$_{\mathrm{P}}$ changes during the variable logic operation of Table 1. The amount of change in $V(G_{M3})$ due to the change is $\Delta V(G_{M3})$. Then, $V(FG_M)$ becomes Equation (6).

$$V(FG_M) = V_{INV} + \frac{C}{C_{TM}} \left(3\Delta V(G_{M3}) - V_{C2} - V_{C3} + V_{inA} + V_{inB} \right) \tag{6}$$

The total capacitance C_{TM} of FG_M becomes Equation (7) using the gate capacity ratio of νCMOS$_{\mathrm{M}}$ and a unit capacitance C.

$$C_{TM} = 7C \tag{7}$$

In this variable logic operation, the values of Equations (5) and (6) are determined in case V_{inA}, V_{inB}, V_{C1}, V_{C2}, and V_{C3} are determined. Furthermore, the output voltage V_{OUT} is determined depending on whether the values of the obtained floating gate voltages $V(FG_P)$ and $V(FG_M)$ exceed the inversion threshold voltage V_{INV} of νCMOSs or not.

4. **FPD (Floating-Gate Potential Diagram).** The output voltage of the circuit is determined the states of HIGH (V_{DD}) or LOW (0 [V]) by the potential of the floating gate. Therefore, the circuit operation is understood in a very straightforward manner by analyzing the variation of $V(FG_M)$ as a function of other parameters such as the input voltages to the multiple input gates and the capacitive coupling coefficients. In Figure 4(a), $V(FG_M)$ of the νCMOS$_{\mathrm{M}}$ in Figure 2 is shown as a function of the principal variable ($V_i = V_{inA} + V_{inB}$). Such representation of Figure 4(a) is called a Floating-Gate Potential Diagram (FPD), and is used very extensively in the design and analysis of νCMOS circuits.

In the variable logic operation of νCMOS$_{\mathrm{M}}$ of the proposed circuit, when V_{inA}, V_{inB}, V_{C2}, V_{C3}, and $V(G_{M3})$ are all V_{DD}, $V(FG_M)$ takes the maximum value of V_{DD}. This represents the upper limit of the FPD ordinate. The baseline represents the change in $V(FG_M)$ when V_{C2}, V_{C3}, and $V(G_{M3})$ are all 0 [V], where $C_{M4} = C_{M5} = C/7$, the maximum of baseline is $2V_{DD}/7$. For example, if (V_{C1}, V_{C2}, V_{C3}) = ("0", "0", "0"), the FPD of FG_M looks like a thick line in Figure 4(a). As $V(FG_M)$ exceeds $V_{DD}/2$ when $(V_{inA}, V_{inB}) = (0, 1)$,

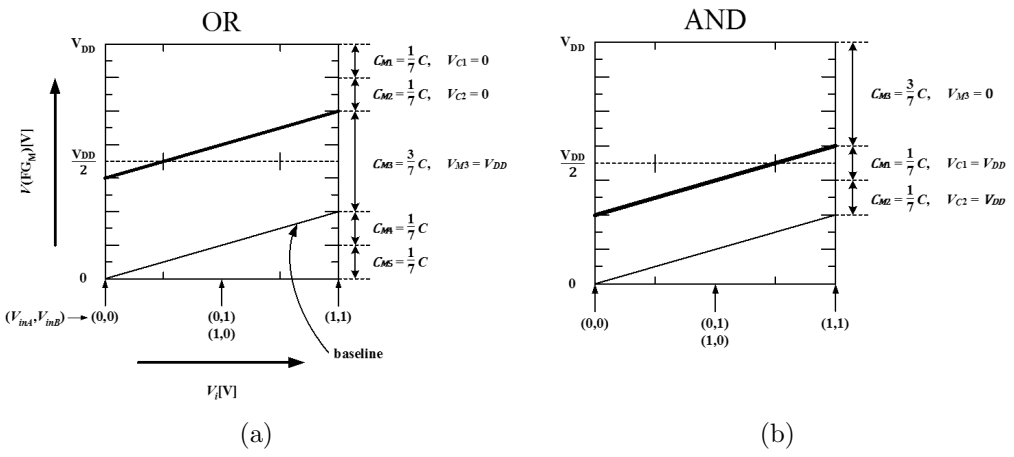

FIGURE 4. FPD (OR, AND)

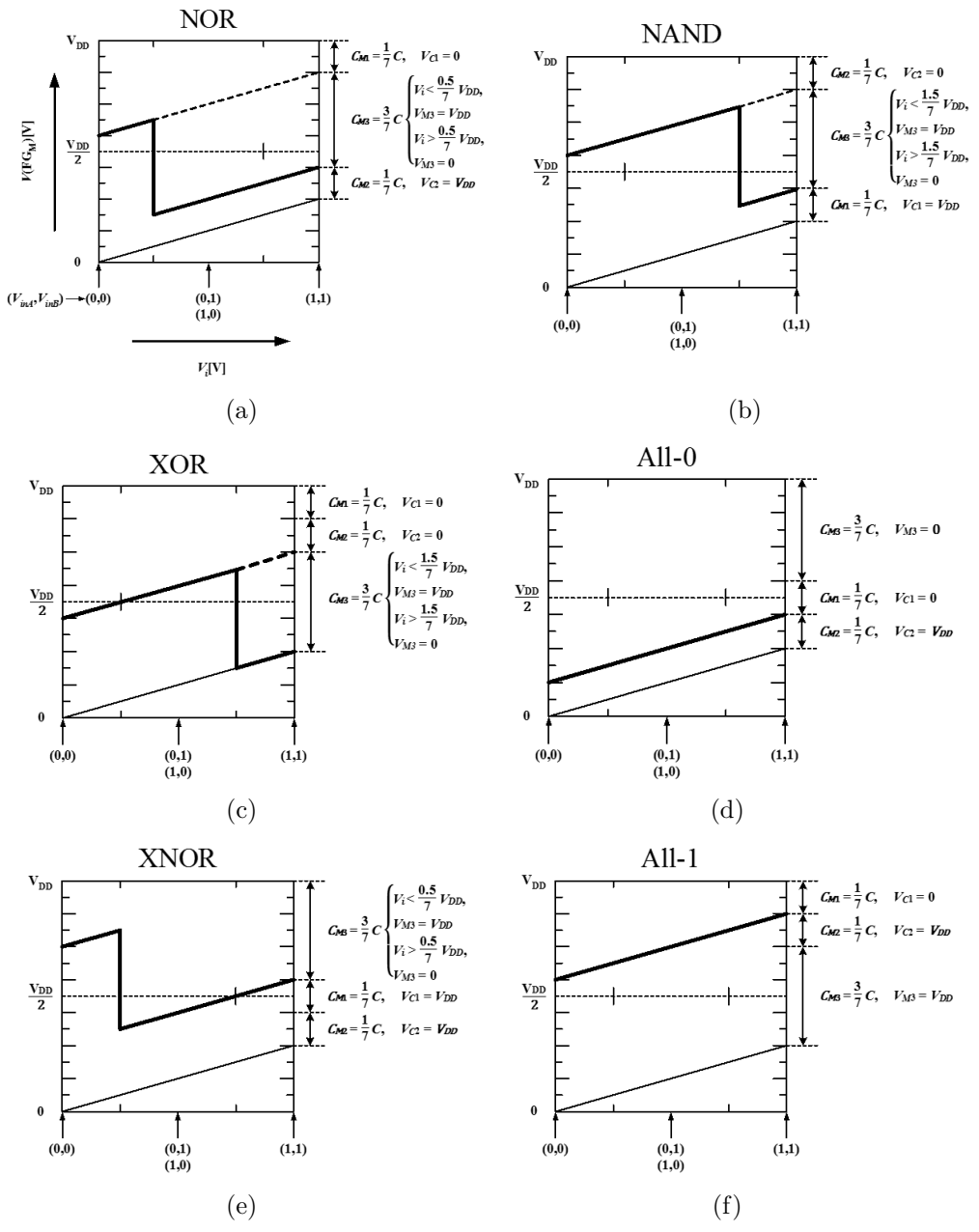

FIGURE 5. FPD (NOR, NAND, XOR, All-0, XNOR, All-1)

$(1,0)$, and $(1,1)$, and $V(FG_M)$ is louted $V_{DD}/2$ when $(V_{inA}, V_{inB}) = (0,0)$, the output in this case can satisfy the logical function of the OR. In another example, if (V_{C1}, V_{C2}, V_{C3}) = ("1", "0", "0"), the FPD of FG_M looks like a thick line in Figure 5(c). As $V(FG_M)$ exceeds $V_{DD}/2$ when $(V_{inA}, V_{inB}) = (0,1)$ and $(1,0)$, and $V(FG_M)$ is louted $V_{DD}/2$ when $(V_{inA}, V_{inB}) = (0,0)$, $(1,1)$, the output in this case can satisfy the logical function of the XOR. Similarly, by switching V_{C1}, V_{C2} and V_{C3}, FPD can be expressed as shown in Figures 4 and 5. Hence eight logical functions can be confirmed from Figures 4 and 5.

5. **Simulation Result.** Figures 6, 7, and 8 show the results of executing HSPICE simulation using the Rohm 0.18 μm process and the device parameters in Table 2 for a 2-input variable logic circuit. In the FG calibration operation in Figure 2, the control signals V_{C1}, V_{C2}, and V_{C3} are set to "1"; furthermore the input signals V_{inA} and V_{inB} are set to "0". Thereafter, when PHASE1 is entered, $V(FG_P)$ is $V_{DD}/2$ as shown in Equation (1). Subsequently, in PHASE2, $V(FG_P)$ slightly increases in voltage as shown in Equation (2).

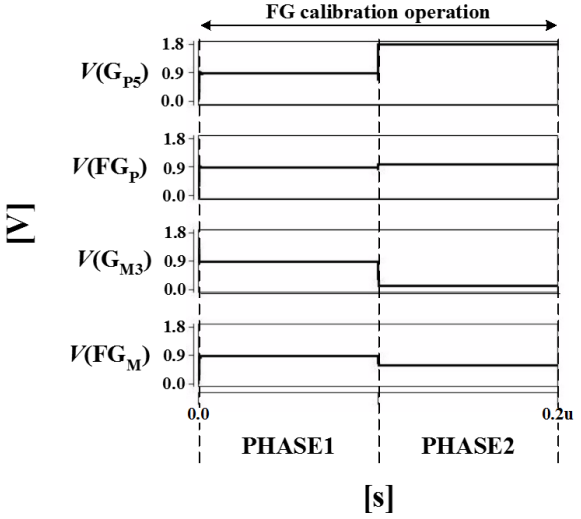

FIGURE 6. Simulation result (potential during FG calibration operation)

Next, variable logic operation will be described. For example, when the input signals (V_{inA}, V_{inB}) are changed to ("1", "1") → ("1", "0") → ("0", "1") → ("0", "0") in case the control signals (V_{C1}, V_{C2}, V_{C3}) are ("1", "1", "1"), the output signal V_{OUT} becomes in the state of "1" → "0" → "0" → "0". This realizes the AND function. Subsequently, when (V_{C1}, V_{C2}, V_{C3}) is changed to ("1", "0", "0") in case (V_{inA}, V_{inB}) are changed in the same manner as above, V_{OUT} changes to a state "0" → "1" → "1" → "0". This realizes the XOR function.

TABLE 2. Device parameters and simulation conditions

Symbol	Description	Value	Units
V_{DD}	Power supply voltage	1.8	V
C	A unit capacitance	16	fF
W_n/L_n	Width/Length of nMOS transistor	1.0/0.18	μm
W_p/L_p	Width/Length of pMOS transistor	3.0/0.18	μm

Similarly, NAND, All-1, XNOR, NOR, All-0, OR can be realized by changing the control signals V_{C1}, V_{C2}, V_{C3}. Matching up the simulation result and the logic function (FPD) shown in Figures 4 and 5 can be confirmed.

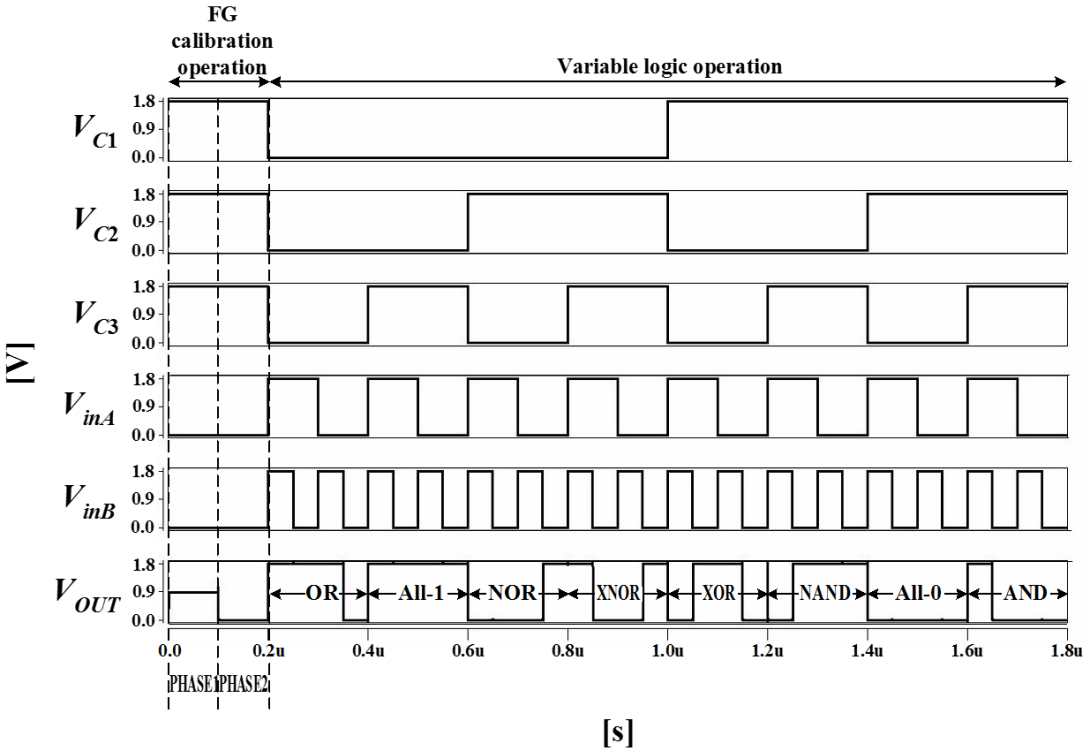

FIGURE 7. Simulation result (logic function)

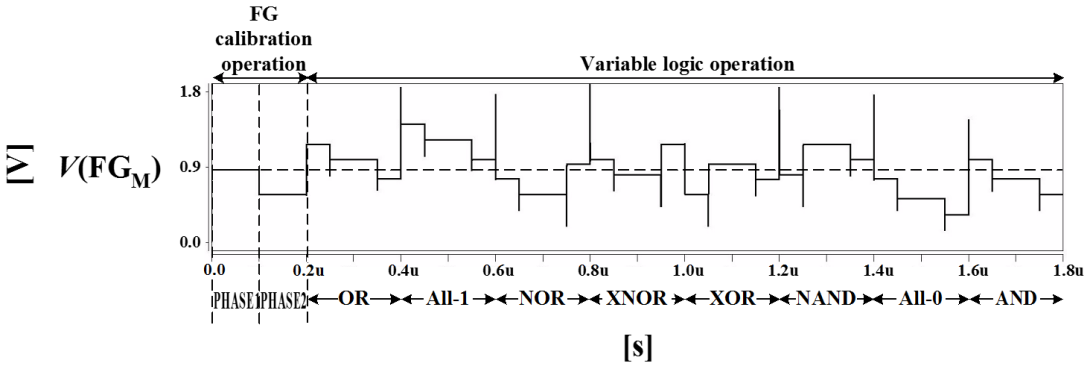

FIGURE 8. Simulation result ($V(FG_M)$)

Furthermore, matching up Figure 7 and Figures 4 and 5 of FPD can be confirmed. From this, being operating as analyzed from the simulation results can be confirmed.

6. **Conclusions.** In this paper, analysis using FPD is made on the νCMOS variable logic circuit with FG calibration. Analysis by FPD clearly showed the output voltage corresponding to the input voltage. Furthermore, from the analysis by FPD and the result of HSPICE simulation, we confirmed that the eight logic functions are currently operating. As a result, we confirmed the properly operating of the circuit. From simulation results, we proved correct the analysis of FPD. In the future, we would like to clarify the design method of variable logic circuits.

Acknowledgment. This work is supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Synopsys, Inc., Cadence Design Systems, Inc., and Rohm Corporation. This work is supported by Tokai University General Research Organization Grant.

REFERENCES

[1] T. Senboku, M. Fukuhara and M. Yoshida, Proposal of a variable logic circuit with a single output terminal using neuron MOS transistors, *The IEICE Transactions*, vol.J87-C, no.8, pp.656-657, 2004.
[2] M. Fukuhara, Y. Suzuki and M. Yoshida, Proposal of a variable logic circuit using neuron MOS transistors, *The IEICE Transactions*, vol.J86-C, no.2, pp.202-203, 2003.
[3] R. Ohtsuka, T. Kurano, N. Onji, K. Yamada and M. Fukuhara, Study of a neuron CMOS variable logic circuit with floating gate calibration, *IEEJ*, 2019.
[4] T. Shibata and T. Ohmi, Neuron MOS binary-logic integrated circuits – Part I: Design fundamentals and soft hardware-logic circuit implementation, *IEEE Trans. Electron Devices*, vol.40, no.3, pp.570-576, 1993.
[5] T. Shibata and T. Ohmi, A functional MOS transistor featuring gate-level weighted sum and threshold operations, *IEEE Trans. Electron Devices*, vol.39, no.6, pp.1444-1455, 1992.
[6] K. Kotani, T. Shibata and T. Ohmi, Neuron-MOS binary-logic circuits featuring dramatic reduction in transistor count and interconnections, *International Electron Devices Meeting (IEDM'92)*, pp.432-434, 1992.
[7] Y. Harada, K. Fujimoto, M. Fukuhara and M. Yoshida, A minimum hamming distance search associative memory using neuron CMOS inverters, *IEEJ Trans. Electronics, Information and Systems*, vol.136, no.1, pp.36-42, 2016.
[8] A. Hideharu, *FPGA Principle and Configuration*, Ohmsha, 2016 (in Japanese).