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ANALYSIS OF CROSS-CONNECTED FIBONACCI SWITCHED CAPACITOR CONVERTER

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Abstract. *As semiconductor technology has advanced, various electric products such as flash memory and LED driver circuits use SCCs (switched capacitor converters) as power converters for them. This trend brings an issue that the higher performance SCCs have, the better quality the products can have. Up until now, many types of SCCs have been suggested. However, most of them are operated by the way that charging and discharging steps are separated. To overcome this, the CCFSCC (cross-connected Fibonacci switched capacitor converter) with its symmetric structure was designed. In this paper, the CCFSCC is analyzed and compared with 2 different SCCs. From the analysis of the CCFSCC, we optimize the sizes of its capacitors and derive its power stage transfer function. Simulation and comparison show that the CCFSCC is confirmed to have high power efficiency, low output ripple voltage and middle circuit size among others.*
Keywords: Switched capacitor converter, Power stage transfer function, Symmetric structure, Optimization of circuit component

1. **Introduction.** With advancement of semiconductor technology, SCC (switched capacitor converter) has been used for various electric products such as USB flash memories [1,2], LED driver circuits [3,4], and RFID product [5,6]. This is because SCCs have no magnetic components like inductors and transformers, which can reduce EMI (electromagnetic interference) and EMC (electromagnetic compatibility) problems as well as its circuit size [7]. This brings an issue that it is important to design an SCC with its high performance in order to improve the qualities of the products.

Since Dickson suggested Dickson SCC [8], many different types of SCCs have been designed: series-parallel type by Mark et al. [9], Fibonacci type by Ueno et al. [10], SCVM (switched capacitor voltage multiplier) type by Chang [11]. These types of SCCs are operated with 2 or 3 operating cycles. During one operating cycle, the steps of charging and discharging capacitors of those SCCs are separated. This requires their high capacitance output capacitors. However, PFSCC (parallel type Fibonacci switched capacitor converter) suggested by Do and Eguchi [12] and CCFSCC (cross-connected type Fibonacci switched capacitor converter) designed by Eguchi et al. [13] are the topology with their symmetric structures. These structures can make SCCs charge and discharge capacitors at the same time for one operating cycle. Also, the symmetric structure can improve the power efficiencies of SCCs and reduce their output ripple voltages. With these reasons, this research selects the CCFSCC as the target topology.

This paper aims to analyze the CCFSCC and compare it with different SCCs. The rest of the paper is as follows. In Section 2, we explain the circuit configuration of the CCFSCC. In Section 3, the CCFSCC is analyzed based on FE model (four-terminal equivalent circuit model) [14,15]. Next, the capacitors of it are optimized and its power

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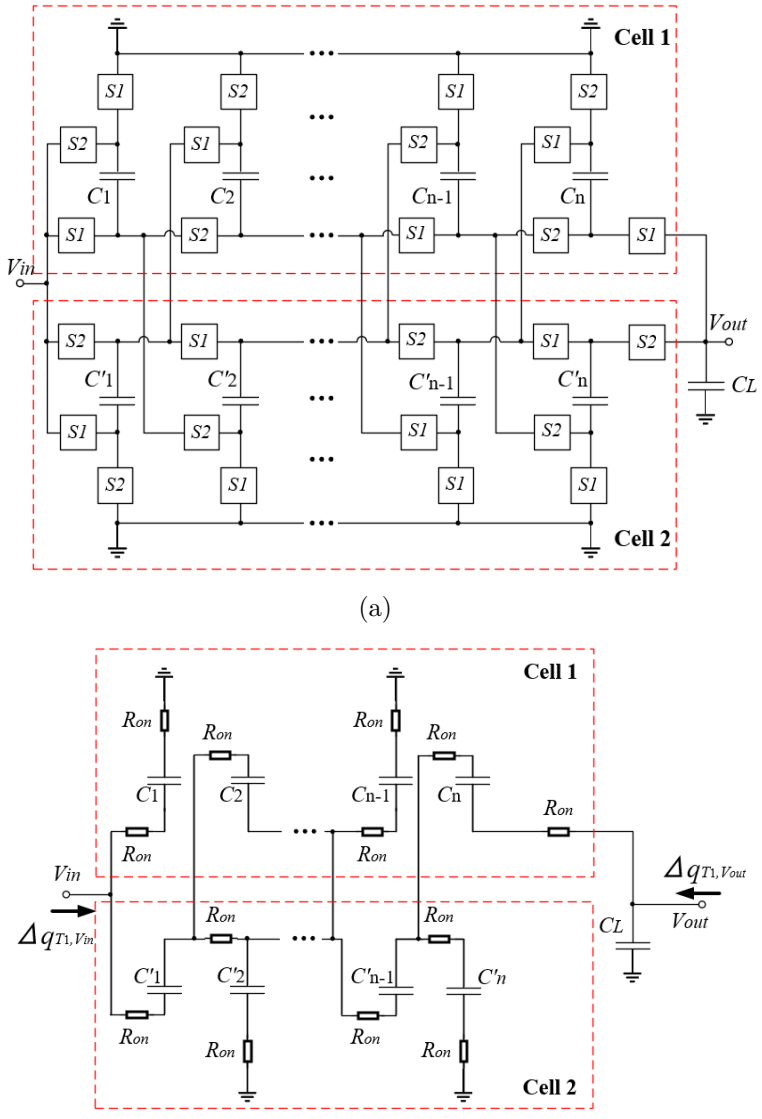
stage transfer function is derived on z-domain. In Section 4, simulations and comparisons are implemented to confirm the performance of the CCFSCC. In Section 5, conclusion and future study are described.

2. **Problem Statement and Preliminaries.** Figure 1(a) shows the CCFSCC (cross-connected Fibonacci switched capacitor converter). In Figure 1(a), S1 and S2 are ideal switches including on-resistors. The CCFSCC consists of two of parallel and cross connected normal FSCCs (Fibonacci switched capacitor converters). With this structural characteristic, the nth capacitors' voltage in each cell of the CCFSCC can be charged up to 2 times compared with that of $(n-1)$th capacitor. The switches are operated inversely with two operating states, following the switching rule as written on Table 1. With this operation, the CCFSCC has symmetric ICEs (instantaneous equivalent circuits). Figure 1(b) shows the ICE at state-1.



(a)

(b)

FIGURE 1. Target circuit (a) cross-connected Fibonacci switched capacitor converter (V_{in}, V_{out}, C_n and C_l are input voltage, output voltage, nth capacitor and output capacitor, respectively), (b) instantaneous equivalent circuits at sate-1 of the CCFSCC (R_{on} is on-resistor of each of switches, $\Delta q_{T1,V_{in}\text{ or }out}$ is charge amount of the input or output at state-1)

TABLE 1. Switching rules

State	*Switches*
1	S1s are turned on and S2s are turned off
2	S2s are turned on and S1s are turned off

3. **Theoretical Analysis.** The analysis in this paper is implemented with the conversion ratio of 4 times in the steady state of the CCFSCC.

3.1. **Four-terminal equivalent circuit model.** To analyze the CCFSCC, we model it into the FE model (four-terminal equivalent circuit model) as shown as Figure 2 [14,15]. The FE model is aimed to derive output resistor, R_{SC}, based on energy consumptions by on resistors of switches, R_{on}. With the output resistor, the maximum power efficiency and output voltage of the targeted converter can be obtained.

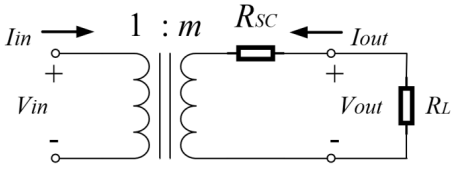


FIGURE 2. Four-terminal equivalent circuit model

By using KCL into the IECs as shown as Figure 3, the relation of the charge amounts of the input, output and capacitors is derived as (1) and (2) at state-1 and -2, respectively.

$$\Delta q_{T1,V_{in}} = \Delta q^1_{T1} - \Delta k^1_{T1}, \quad \Delta k^{n-1}_{T1} = -\Delta k^n_{T1} + \Delta q^n_{T1}, \quad \Delta q_{T1,V_{out}} = \Delta q^1_{T1} - \Delta q^{out}_{T1} \quad (1)$$

where $\Delta q_{T1,V_{in}}$ and $\Delta q_{T1,V_{out}}$ are the charge amounts of the input and output, Δq^u_{T1} (cell 1) and Δk^u_{T1} (cell 2) are the charge amounts of uth capacitors and Δq^{out}_{T1} is the charge amount of the output capacitor at state-1.

$$\Delta q_{T2,V_{in}} = \Delta k^1_{T2} - \Delta q^1_{T2}, \quad \Delta q^{n-1}_{T2} = -\Delta q^n_{T2} + \Delta k^n_{T2}, \quad \Delta q_{T2,V_{out}} = \Delta k^n_{T2} - \Delta q^{out}_{T2} \quad (2)$$

where $\Delta q_{T2,V_{in}}$ and $\Delta q_{T2,V_{out}}$ are the charge amounts of the input and output, Δq^u_{T2} (cell 1) and Δk^u_{T2} (cell 2) are the charge amounts of uth capacitors at state-1 and Δq^{out}_{T2} is the charge amount of the output capacitor.

By using (1) and (2), the charge amount relation between the input and output is given as (3). From (3), the conversion ratio, m, is 2^n.

$$\Delta q_{V_{in}} = -m\Delta q_{V_{out}} = -2^n \Delta q_{V_{out}}, \quad (3)$$

where $\Delta q_{V_{in}}$ and $\Delta q_{V_{out}}$ are the charge amount of the input and output during one operating cycle.

To derive R_{SC} of the CCFSCC, the consumed power by on resistors of switches, W_{T1} is calculated as (4) at state-1. $T1$ and $T2$ are the period at state-1 and 2, respectively.

$$W_{T1} = \left\{ \left(2^{2n-2} R_{on}\right) / T1 \right\} \left(\Delta q^{out}_{T1}\right)^2. \quad (4)$$

Because the CCFSCC has the symmetric IECs, the consumed power by on resistors of switches at state-2, W_{T2}, is equal to W_{T1}, leading the total consumed power during one operating cycle as (5).

$$W_T = W_{T1} + W_{T2} = \left\{ \left(2^{2n} R_{on}\right) / T \right\} \left(\Delta q^{out}_{T1}\right)^2, \quad (5)$$

where with the duty ratio of 50%, $T1$ and $T2$ are the same.

From (5), R_{SC} of the CCFSCC is given as (6).

$$R_{SC} = 2^{2n} R_{on}. \quad (6)$$

Using R_{SC} the output voltage and the power efficiency, η, can be calculated as (7)

$$V_{out} = \eta V_{in} = \{R_{SC}/(R_L + R_{SC})\}\, V_{in}. \tag{7}$$

3.2. **Capacitor optimizing.** In Section 3.2 and Section 3.3, we set up the conversion ratios of 4 times. Figure 3 shows the ICEs at the conversion ratio of 4 times. According to the charge conservation law, during one operating cycle, the total charged and discharged charge amount in flying capacitors should be equal to that of the output capacitor. This is expressed as (8).

$$2\{C_f(1/4)V_{out} + C_f(1/2)V_{out}\} - 2C_f(V_{out} - V_{in}) = C_L \Delta V_{out}, \tag{8}$$

where C_f and C_L are the capacitances of flying capacitors and the output capacitor and, ΔV_{out} is the output ripple voltage of the output.

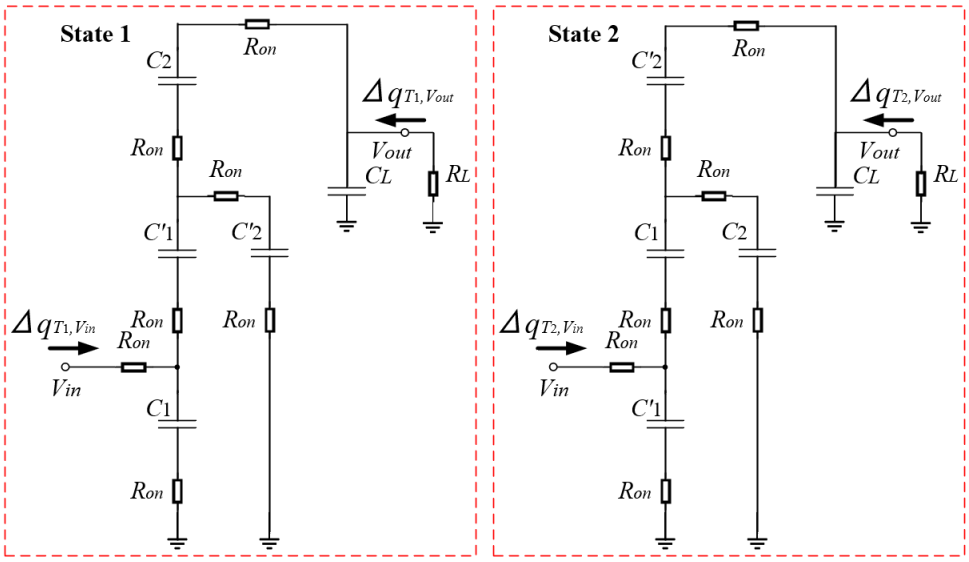


FIGURE 3. Instantaneous equivalent circuits of CCFSCC with 4 times conversion ratio

When the output voltage is much higher than the output ripple voltage, the transferred energy, E_{tran}, from flying capacitors to the output capacitor can be approximately expressed as (9) [16].

$$E_{tran} \cong C_L V_{out} \Delta V_{out}. \tag{9}$$

For one operating cycle, the transferred energy and the energy consumed by the load should be equal as (10).

$$E_{tran} = (V_{out})^2/(R_L f), \tag{10}$$

where f is the operating frequency as the reciprocal of T.

By using (8)-(10), the capacitances of flying capacitors and the output capacitor can be determined as (11) and (12).

$$C_f = V_{out}/\{2R_L \cdot f \cdot (8V_{in} - 5V_{out})\}. \tag{11}$$

$$C_L = V_{out}/(R_L \cdot f \cdot V_{out}). \tag{12}$$

3.3. **Transfer function.** With consideration for analyzing the CCFSCC on z-domain, the power stage transfer function of it is directly modeled on z-domain.

In the IECs in Figure 3, during one operating cycle, the flying capacitors are connected in parallel to the output port with the output capacitor and the load. Therefore, the charged charge, Q_{charge}, at $(n-1)T$ is derived (13).

$$Q_{charge} = 2\left\{C_f\left(\frac{1}{4}\right)V_{out}((n-1)T) + C_f\left(\frac{1}{2}\right)V_{out}((n-1)T) + C_L V_{out}((n-1)T)\right\}. \tag{13}$$

After the capacitors discharge the charges during one operating cycle, the remained charge in the capacitors at nT, Q_{disch}, is given as (14).

$$Q_{disch} = 2\left\{C_f(V_{out}(nT) - V_{in}(nT)) + C_L V_{out}(nT)\right\}. \tag{14}$$

The current flowing from capacitors to the output port and the current flowing to the load should be equal, leading to (15).

$$(Q_{charge} - Q_{disch})/T = (V_{out}((n-1)T) - V_{out}(nT))/R_L. \tag{15}$$

By substituting (13) and (14) into (15), (16) is given.

$$\begin{aligned} &\left(\frac{3}{2}C_f + C_L\right)V_{out}((n-1)T) + (-2C_f - 2C_L)V_{out}(nT) + 2C_f V_{in} \\ =\ &\frac{(V_{out}((n-1)T) - V_{out}(nT))}{R_L}. \end{aligned} \tag{16}$$

By transferring (16) in z-domain, the power stage transfer function of the CCFSCC is derived as (17).

$$\frac{V_{out}}{V_{in}} = 2C_f \Bigg/ \left[\left\{-\left(\frac{3}{2}\right)C_f - 2C_L + \left(\frac{T}{R_L}\right)\right\}z^{-1} + \left\{2C_f + 2C_L + \left(\frac{T}{R_L}\right)\right\}\right]. \tag{17}$$

4. **Simulation and Comparison.** To confirm the performance (power efficiency and output ripple voltage) of the CCFSCC, it is simulated with the condition written in Table 2. This condition can lead the SCCs to be operated with its high efficiency and without consideration of its operating frequency. Also, different types of SCCs are simulated with the same condition in order to compare the CCFSCC with them.

Table 2. Simulation conditions

Parameter	Values
R_{on}	0.1Ω
R_L	1kΩ
T	1μs
C	10μF
D	0.5
V_{in}	10V

Figure 4 shows that as the conversion ratio increases, the power efficiency of the CCFSCC is the highest among 3 different SCCs. This results from the performance of the CCFSCC that it has the smallest R_{SC}.

Figure 5 describes that the SCC with the second lowest output ripple voltage is the CCFSCC. This is because with the symmetric construction, the CCFSCC can charge and discharge capacitors at the same time during its operating cycle.

The number of circuit components at different conversion ratios is shown in Figure 6. The CCFSCC is the middle circuit size at the conversion ratio of 2 to 16 times because it is based on combining two FSCCs.

5. **Conclusions.** In this paper, the CCFSCC has been analyzed, simulated and compared. Through theoretical analysis of the CCFSCC, the way to select the capacitances of its flying capacitors and output capacitor is derived. The transfer function is also induced on z-domain. This will be utilized to design the digital controller of the CCFSCC. The comparison with 2 different types of SCCs shows that the CCFSCC has the highest power efficiency with middle circuit size of it on average. It is confirmed that the CCFSCC can be a solution when a target system requires the low output ripple voltage and the high power efficiency without consideration of its size.

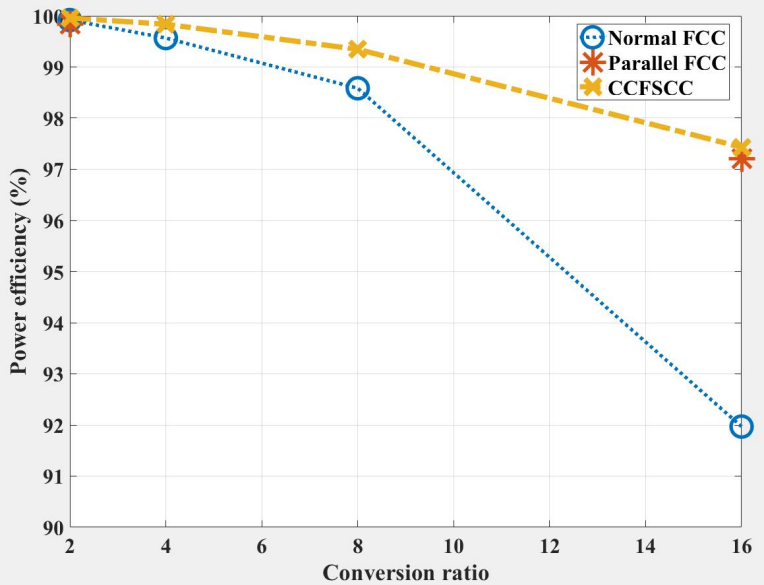


FIGURE 4. Simulated power efficiencies of SCCs

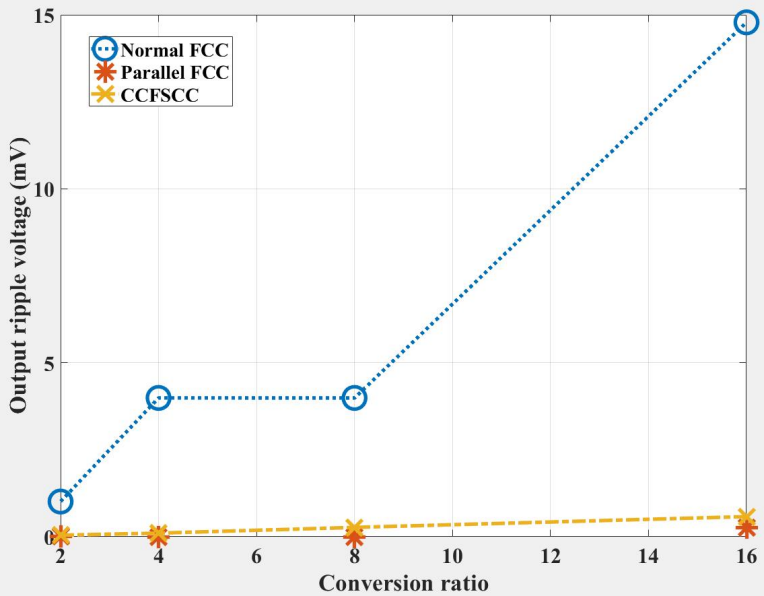


FIGURE 5. Simulated output ripple voltages of SCCs

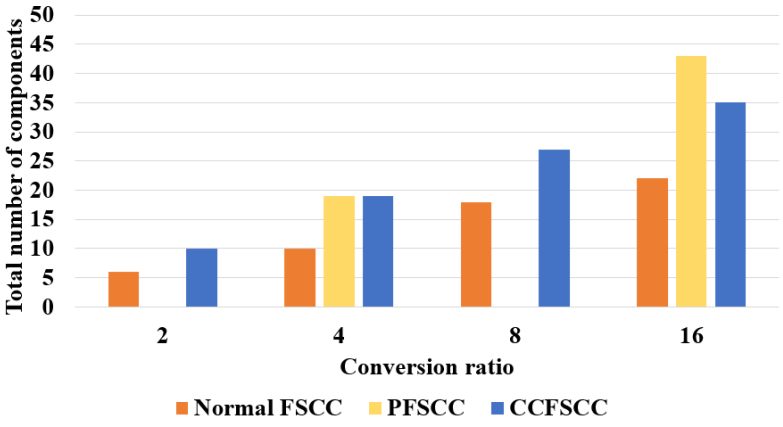


FIGURE 6. The number of circuit components consisting of switches and capacitors

A future study is as follows: to optimize different parameters such as the operating frequency of CCFSCC, to design its controller and to design its hardware.

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