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A FLASH TYPE A/D CONVERTER USING NEURON CMOS INVERTERS WITH THRESHOLD COMPENSATION CIRCUITS

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Abstract. *An A/D converter is used to convert an analog signal to a digital signal. Among others, a flash type A/D converter which converts the analog signal to the digital signal at once is generally used for high-speed applications. However, depending on the increase of the resolutions, the number of comparators rapidly increases, and the power consumption of the A/D converter increases. In this study, we propose a flash type A/D converter using neuron CMOS inverters with threshold compensation circuits. The proposed circuit is not affected by the fluctuation of the threshold voltage of the neuron CMOS inverter and parasitic capacitance. Furthermore, the proposed circuit can achieve lower power consumption characteristics and higher operation speed than the conventional A/D converter. The characteristics of the proposed circuit are clarified by HSPICE simulations.*

Keywords: A/D converter, Flash type, Neuron CMOS inverter

1. **Introduction.** An analog-to-digital converter (A/D converter) is used to convert an analog signal to a discrete signal. In the A/D converters, there are several kinds of circuit configurations, such as flash type, delta-sigma type and double integrating type depending on a wide range of applications. Among others, the flash type A/D converter which converts the analog signal to the digital signal at once is generally used for high-speed applications [1,2]. The A/D converter with n-bit resolution, which converts the analog signal to the n-bit digital signal judges the voltage levels by comparing between an analog input voltage with reference voltages generated by a resistor radder circuit. In conventional methods, the $2^n - 1$ analog comparators with high power consumption are necessary for realizing the n-bit flash type A/D converter. Therefore, depending on the increase of resolutions, the number of the analog comparators increases exponentially and the power consumption of the flash type becomes very large.

To solve this problem, we have already proposed a flash type A/D converter using neuron CMOS (complementary metal-oxide-semiconductor) inverters which has a low power consumption characteristic and a small circuit scale [3,4]. The A/D converter judges the voltage levels and coverts the analog signal to the digital signal at a high-speed

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by utilizing a variable threshold voltage characteristic of the neuron CMOS inverter [5]. However, there is a problem that the threshold voltage of the neuron CMOS inverters may fluctuate by ambient temperature and variation in a manufacturing process. In the previous research, malfunctions are caused by this fluctuation and parasitic capacitances between input terminals of the neuron CMOS inverters and substrate.

In this study, we propose a flash type A/D converter using neuron CMOS inverters with threshold compensation circuits for solving these problems. In the proposed flash type A/D converter, the floating gate voltage of the neuron CMOS inverters is equal to the threshold voltage. After that, the floating gate voltage lowers in proportion to reference voltages generated by a resistor radder circuit. Finally, by adding an analog input voltage to the neuron CMOS inverters, the floating gate voltage increases, and the neuron CMOS inverters judge the voltage levels depending on whether the floating gate voltage reaches the threshold voltage. By the above-mentioned operations, the proposed circuit can convert the analog signal to the digital signal without the influence of the fluctuations of the threshold voltage. Furthermore, in this study, we designed the proposed A/D converter by using ROHM Semiconductor 0.18 μm CMOS process. In HSPICE simulations of the proposed circuit, we confirmed that expected results are obtained.

2. **Circuit Configuration.** Figure 1 illustrates a circuit configuration of the flash type A/D converter using neuron CMOS inverters with threshold compensation circuits in the

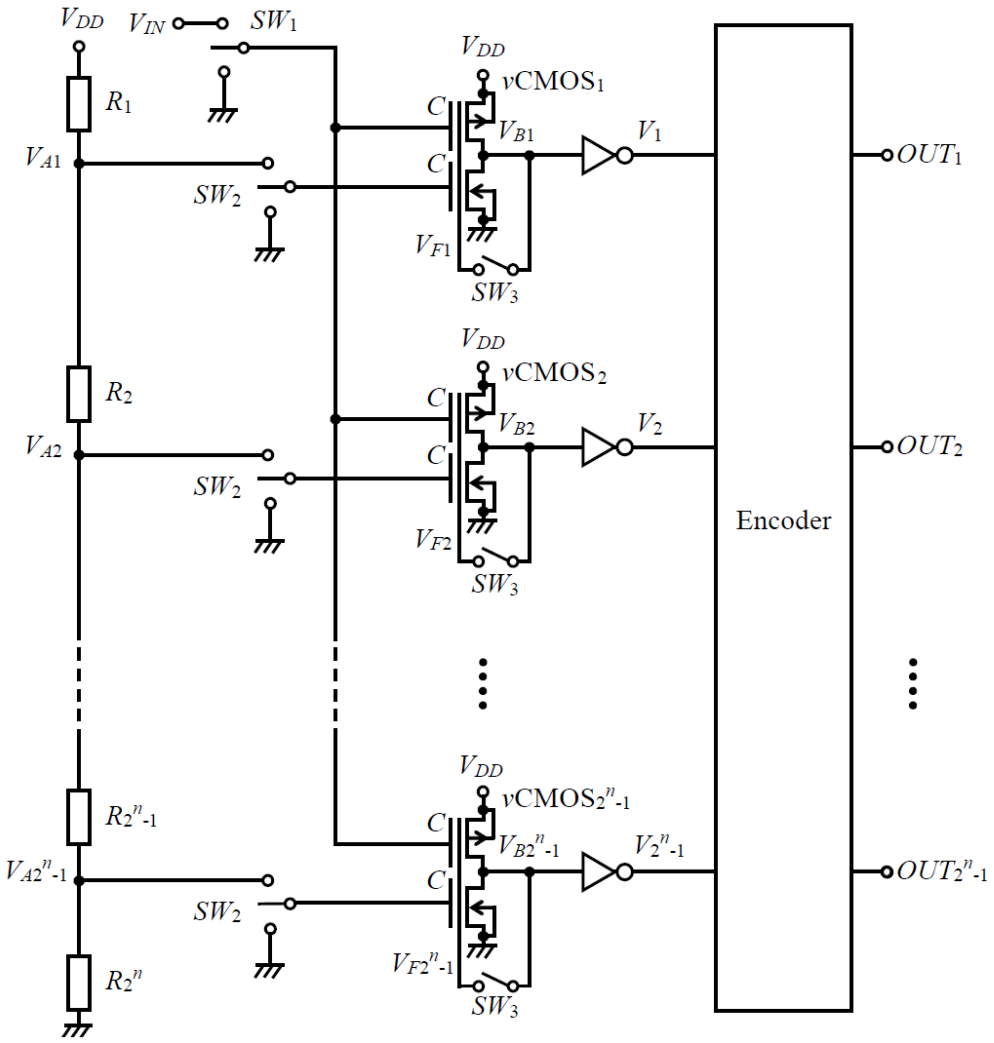

FIGURE 1. Circuit configuration of the flash type A/D converter using neuron CMOS inverter with threshold compensation circuit

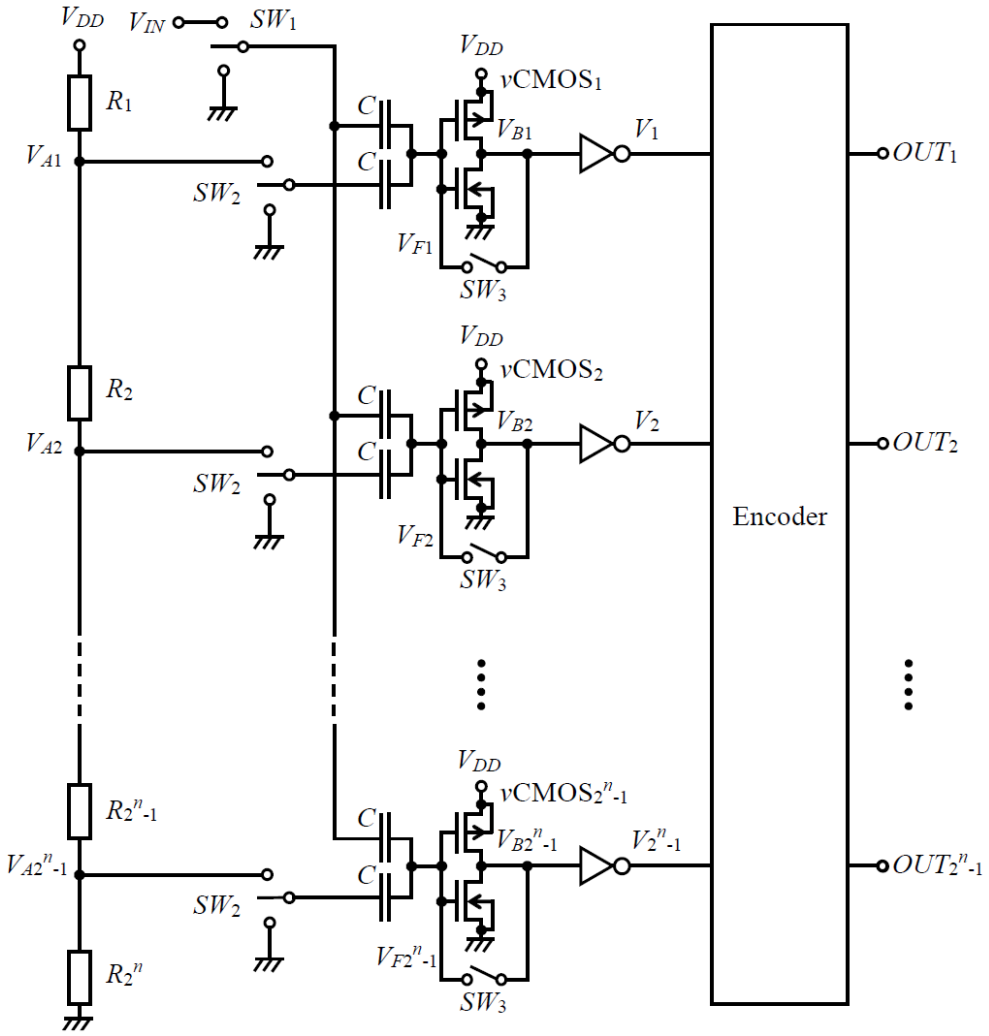

FIGURE 2. Equivalent circuit of the proposed A/D converter

case of the n-bit resolution. Figure 2 shows an equivalent circuit of the proposed flash type A/D converter. In this figure, V_{DD} is a supply voltage, $\nu\mathrm{CMOS}_i$ $(i = 1, 2, \ldots, 2^n - 1)$ is the neuron CMOS inverter, V_{IN} is an analog signal, V_{Fi} is a the floating gate voltage of the neuron CMOS inverter, and V_{Ai} is a reference voltage generated by the resistor radder circuit with R_j $(j = 1, 2, \ldots, 2^n)$. When all resistances R_j are designed to equal, the reference voltage V_{Ai} is expressed as follows:

$$V_{Ai} = V_{DD} - \frac{V_{DD}}{2^n} i. \tag{1}$$

We will describe the operation principle of the proposed A/D converter. First, for preparing the threshold compensation, SW_1 is connected to GND, and SW_2 are connected to the reference voltage V_{Ai}. When SW_3 becomes "ON", an output terminal is connected to an input terminal of the neuron CMOS inverter. In this timing, the floating gate voltage V_{Fi} of the neuron CMOS inverter is expressed as:

$$V_{Fi} = V_{TH}, \tag{2}$$

where, V_{TH} is the threshold voltage of the neuron CMOS inverter.

Next, when the SW_3 becomes "OFF" and the SW_2 is connected to GND, the i-th floating gate voltage V'_{Fi} of the neuron CMOS inverter $\nu\mathrm{CMOS}_i$ is expressed by following equation:

$$V'_{Fi} = V_{TH} - \frac{V_{Ai} C}{C_T}, \tag{3}$$

where, C denotes a unit capacitance, and C_T is the total of capacitances of C between the input terminal and the floating gate of neuron CMOS inverter and parasitic capacitance C_0 between the input terminal and substrate. The total capacitance C_T of the neuron CMOS inverter is expressed as:

$$C_T = 2C + C_0. \tag{4}$$

From these equations, we can see that the floating gate voltage decreases in proportion to the reference voltage.

Finally, when the SW_1 is connected to the analog signal V_{IN}, the floating gate voltage V''_{Fi} is shown as follows:

$$V''_{Fi} = V_{TH} - \frac{V_{Ai}C}{C_T} + \frac{V_{IN}C}{C_T}. \tag{5}$$

The output V_{Bi} of the neuron CMOS inverter becomes 0 or V_{DD} depending on whether the floating gate voltage is higher than the threshold voltage, and V_{Bi} is shown as:

$$V_{Bi} = \begin{cases} V_{DD} & \left(V_{TH} \geq V_{TH} - \dfrac{V_{Ai}C}{C_T} + \dfrac{V_{IN}C}{C_T}\right) \\ 0 & \left(V_{TH} < V_{TH} - \dfrac{V_{Ai}C}{C_T} + \dfrac{V_{IN}C}{C_T}\right) \end{cases}. \tag{6}$$

By organizing this equation, the output V_{Bi} is expressed as:

$$V_{Bi} = \begin{cases} V_{DD} & (V_{Ai} \geq V_{IN}) \\ 0 & (V_{Ai} < V_{IN}) \end{cases}. \tag{7}$$

From these equations, we can confirm that the analog signal V_{IN} is compared with the reference voltage V_{Ai}, and the output of the neuron CMOS inverter is changed by voltage magnitude of the analog signal and the comparison reference voltage. Furthermore, we can see that the proposed circuit is not affected by the fluctuation of the threshold voltage V_{TH} and the parasitic capacitance C_0.

The output V_{Bi} of the neuron CMOS inverter, i.e., quantized signal, is shaped by the inverters. Finally, the shaped signals are added to an encoder, and binary signals are outputted. For these operations, we can confirm that the proposed circuit can judge the voltage levels of the analog signal. Also, the proposed circuit can perform A/D conversion exactly, because the fluctuation of the threshold voltage and parasitic capacitances can be ignored. Furthermore, we can easily configure the proposed circuit, and the circuit scale of the proposed circuit is small as same as that of the conventional A/D converter using neuron CMOS inverters.

3. **Simulation.** To clarify the characteristics of the proposed flash type A/D converter with 6-bit, HSPICE simulations were performed by using ROHM Semiconductor 0.18 μm CMOS process. Table 1 shows the summary of the parameter name and its value in the simulation. In these simulations, the supply voltage V_{DD} was applied 1.8 V, and the resistances R_i $(i = 1, 2, \ldots, 64)$, the capacitance C, and the MOS transistors were designed according to the value of this table.

Figure 3 demonstrates the simulated results of the floating gate voltage V_{Fi} of the neuron CMOS inverter in the threshold voltage compensation operation. In this simulation, we can confirm that the floating gate V_{Fi} decreases in proportion to the reference voltage as shown in Equations (2) and (3) after the floating gate voltage V_{Fi} becomes equal to the threshold voltage. The proposed circuit is not affected by the fluctuation of the threshold voltage and the parasitic capacitances, because the floating gate voltage decreases in proportion to the reference voltage without these affections and the floating gate voltage is used by the A/D conversion.

TABLE 1. Device parameters of the proposed circuit for the simulations

Parameter name	Value
Supply voltage V_{DD}	1.8 V
Resistance R_i $(i = 1, 2, \ldots, 64)$	1 kΩ
Capacitance C	16 fF
Channel length of p-channel MOS transistor	0.18 μm
Channel width of p-channel MOS transistor	3.9 μm
Channel length of n-channel MOS transistor	0.18 μm
Channel width of n-channel MOS transistor	1 μm

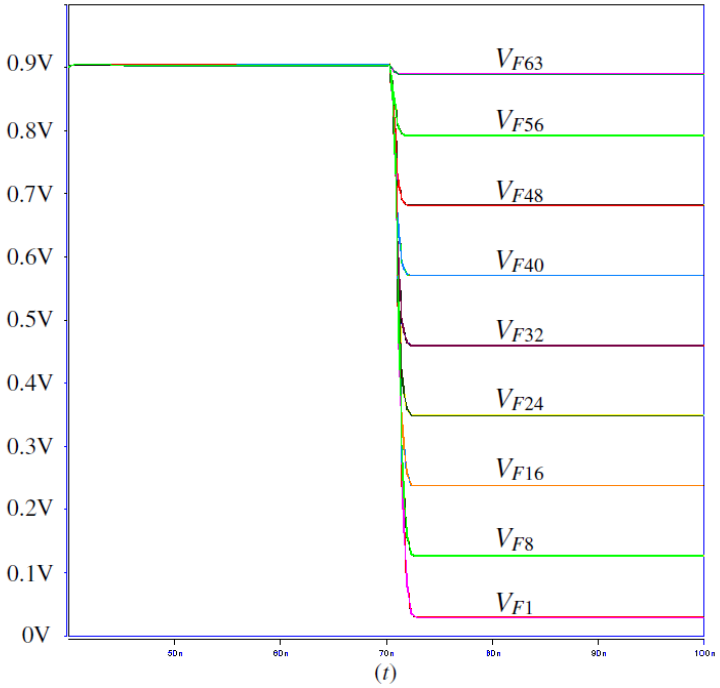

FIGURE 3. Simulated waveforms of the floating gate voltage of the neuron CMOS inverters

Figure 4 shows the simulated results of several outputs of the floating gate voltage V_{Bi} of the neuron CMOS inverter. In this simulation, we can confirm that the proposed circuit judges 64 stages of the voltage level of the analog signal, triangle wave, at same intervals.

In the case of the 6-bit proposed A/D converter, we have also confirmed the operation up to the clock conversion frequency 910 MHz. Also, the power consumption of the proposed circuit is 6.2 mW. From these results, we confirmed that performance in the operation speed and the power consumption same as the conventional A/D converter using the neuron CMOS inverters can be obtained by the proposed circuit. Furthermore, we confirmed that the proposed circuit can achieve the expected results even the channel width of the transistors of the neuron CMOS inverters has 10% variation.

4. **Conclusion.** In this paper, we proposed the flash type A/D converter using neuron CMOS inverters with threshold compensation circuits. In the conventional A/D converter using the neuron CMOS inverters, there are problems that the malfunction occurs by the fluctuation of the threshold voltage and parasitic capacitances. By operating A/D conversion after threshold compensation operation, the proposed circuit can convert the analog signal to the digital signal without the effect of these errors. Furthermore, the circuit configuration is simple, because the proposed circuit can be constituted by adding a little change to the conventional circuit.

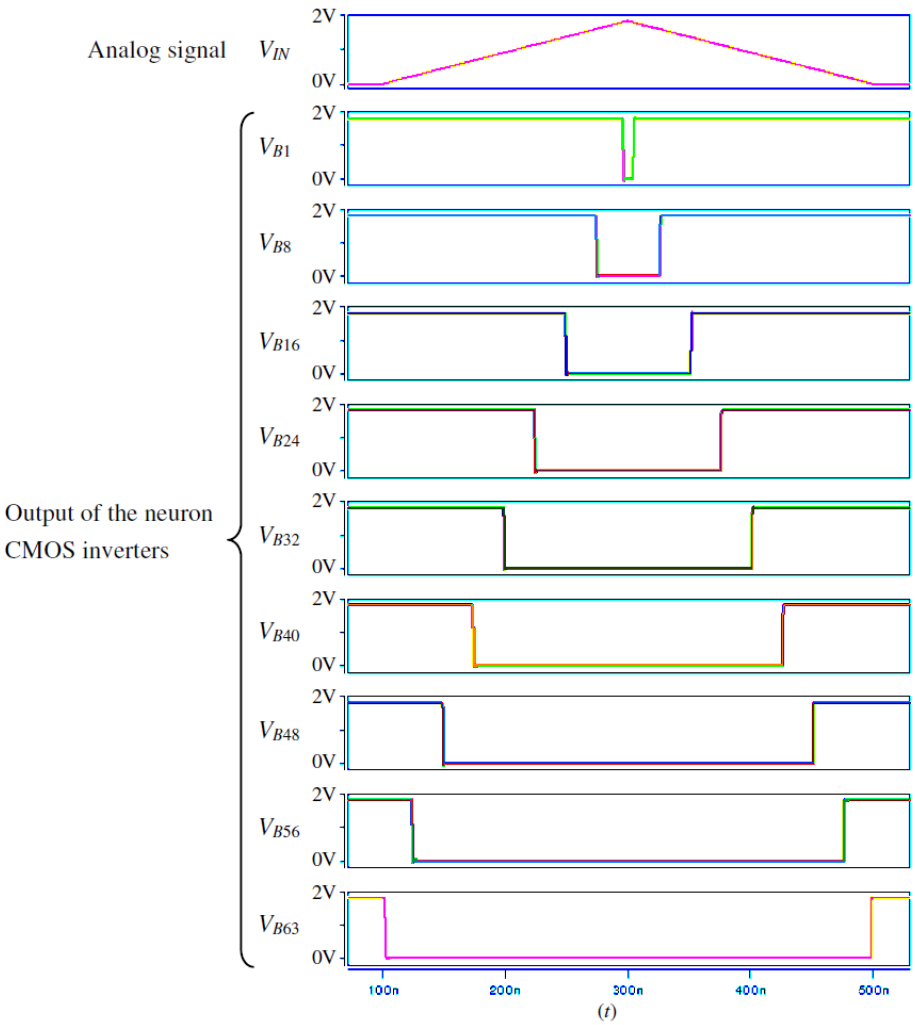

FIGURE 4. Simulated waveforms of the output of the neuron CMOS inverters

We confirmed the expected results through HSPICE simulations. In the simulations, the clock conversion frequency was 910 MHz when the resolution was 6-bit, and the power consumption was 6.2 mW.

In a future study, we are going to integrate the proposed flash type A/D converter into an IC chip, and confirm the effectiveness of the IC chip through the experiments.

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