

PRODUCTION PLANNING FOR LED WAFER FABRICATION AND CHIP PACKAGING WITH LAGRANGIAN RELAXATION HEURISTICS

JUNE-YOUNG BANG¹ AND BONGJOO JEONG^{2,*}

¹Department of Industrial and Management Engineering
Sungkyul University
53, Seonggyeoldae-hak-ro, Manan-gu, Anyang-si, Gyeonggi-do 14097, Korea
jybang@sungkyul.ac.kr

²Department of Business Administration
Kongju National University
56, Gongjudaehak-ro, Gongju-si, Chungcheongnam-do 32588, Korea

*Corresponding author: jbj@kongju.ac.kr

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ABSTRACT. *In this paper, we propose Lagrangian relaxation heuristics to obtain near optimal production plan for LED wafer fabrication and chip packaging. In the front-end process of the LED manufacturing, wafers are fabricated with circuit patterning. In this process, product type of wafers is determined by their die sizes, and wave length of emitting light. In the backend process, the wave length can be adjusted by applying a fluorescent substance on the surface of LED dies. The product types are binned according to the wave length, and this binning is not stabilized and overlapped with different product types of wafer fabrication. Therefore, the production plan, determining release quantity of wafers and chips to production, should be recalculated quickly enough in the case that the binning ratio becomes greatly disturbed to meet the customers' demand. Results of computational tests showed that the near optimal production plan can be obtained within a half hour, while the optimal solution can be obtained around 2 hours CPU time with a commercial solver. The percentage gap between optimal and Lagrangian heuristics is less than 5% for the single period problem.*

Keywords: Production planning, Lagrangian relaxation heuristics, LED, Mixed integer programming, Wafer fabrication, Chip packaging

1. Introduction. In this paper, we suggest an efficient production planning approach for the 2-stage production system in which manufacturing technology is not mature such as the light-emitting diode (LED) industry. In the production process, the silicon wafer as raw material can be finished into multiple types of final product. Even though the production is made for the specific target final product, the resulting production would result in production of the similar types of products as well as the final product. Therefore, the production planning in the production system with immature production technology should be more sophisticated to reduce the production costs caused by the mismatch of production and demand.

In general, a large complex production system consists of successive subsystems. As the complexity of the production system increases, the elapsed time for factory production planning also exponentially increases. To reduce the time required to create a factory production plan, you can divide the entire production system into multiple subsystems and generate a factory production plan for each subsystem independently. In this case, the factory production plan of each subsystem should satisfy the demand or the required

amount from the post-subsystem by considering the relationship of the pre and post process.

In a production system consisting of two production factories as shown in Figure 1, the factory production plan of the factory #2 is first generated with objective of satisfying the customers' demands and calculating the required amount needed to be produced from factory #1. This required amount can be regarded as the demand for the factory #1, and with this demand, the production plan for factory #1 is generated.

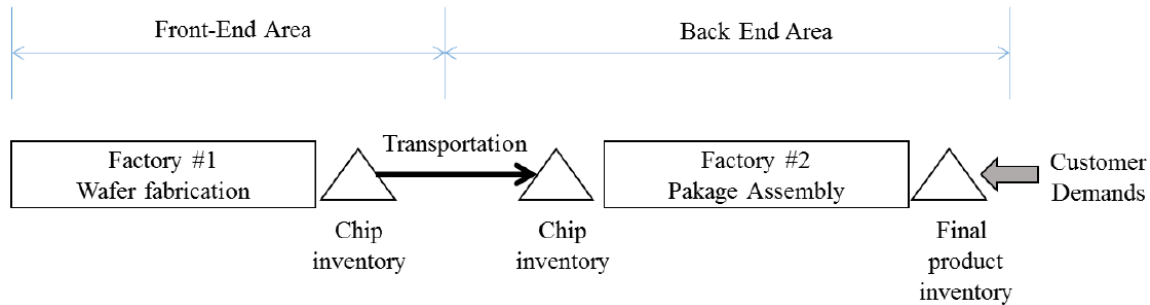


FIGURE 1. Production process of LED manufacturing system

This method for production plan generation is suitable for the industry in which the production technology is stabilized so that the demand and production is steady and forecastable. However, the mismatch of the production plan between the two factories becomes serious in the industries where the production technology is not stabilized like the LED industry and the quality of the product is fluctuating. The characteristics of the LED device are determined by the wave length (= color) and intensity of the light. The structure of the LED product is multi-way tree structure with many nodes and arcs, and the production process path for producing the final product is various. Even if the raw material is requested to be produced in a good yield (production ratio) in factory #2, the product cannot be produced due to a low yield (production ratio) in the factory #1, and excessive by-products can be produced to produce the required produce from factory #2. Due to the high yield variability of LEDs, the production plan should be recalculated instantly according to the changed throughput. The purpose of this study is to obtain near-optimal production plans for complex production systems within a reasonably short time.

Many researchers have been focused on scheduling problems for wafer fabrication facilities. However, only a few researches are published for scheduling problem for the LED wafer fabrication and packaging process. Liu and Chang [4] suggested an approach for production scheduling of flexible flow shops with significant sequence-dependent setup effects. Shiang et al. [6] developed simulation model of the LED sorting process which is in the end of the fabrication, and suggested heuristic scheduling method for the LED die sorting. Sung et al. [7] proposed inventory management policy for LED production with the uncertainty. Zhang et al. [9] developed an open queue approximation model for a wafer fabrication system and then used the low-fidelity estimates of lead times obtained from the approximation model in a recently developed multi-fidelity simulation optimization method.

The lot transfer problem between multi-facilities is similar to the multi-level capacitated lot-sizing problem (MLCLP). In MLCLP, the lots-sizes must be determined for multi-level production inventory systems with capacity constraints on the production facilities. Brahimi et al. [2] thoroughly reviewed the single time lot-sizing problems for uncapacitated and capacitated versions. Trigerio et al. [8] developed a promising heuristic to solve large-scale capacitated lot-sizing problems based on Lagrangian approach. Lin and Chen [5] proposed a mathematical model of a multi-stage and multi-site production

planning problem based on TFT-LCD industry. Aghezzaf [1] proposed a mixed integer programming model for mold transfer problem between plants, and developed a linear programming-based heuristic that combines Lagrangian relaxation and linear programming duality for solving the problems. Recently, Jung and Kim [3] developed variable neighborhood search (VNS) algorithm for the two-stage assembly flow shop scheduling problem.

In this research, we propose Lagrangian relaxation heuristics to obtain near optimal production plan for LED wafer fabrication and chip packaging. Computational experiments are done to evaluate performance of the proposed planning method compared with a commercial optimizing tool, CPLEX. This paper is organized as follows. In the next section, the problem in this study is described in more detail with a mathematical formulation. Then, we suggest Lagrangian heuristic algorithms for the problem. To evaluate performance of the algorithms, computational experiments are performed and results are reported. Finally, we conclude the paper with recommendation for future studies of the problem in this study.

2. Problem Descriptions. We now develop a mixed integer programming model (MIP) for determining a single period production plan that minimizes the total cost while meeting the demand as possible. It determines how many wafers of each type and packages with each recipe are released for wafer fabrication and packaging stages.

We consider an LED production line processing 4-inch wafers. Note that up to 2000 chips can be produced from a 4-inch wafer. In this problem, we determine the input quantity of each type of wafers in a wafer fabrication (FAB) and the input quantity of each type of chips in a packaging (PKG) stage. The following assumptions are made in this research (based on situations of a real LED manufacturing system).

- 1) The covered process ranges from FAB to PKG.
- 2) The test process is not considered because its operation time is much shorter and its cost is much cheaper than those of FAB and PKG stages.
- 3) Different types of chips can be produced from a wafer, and also, different packages can be produced from the same chip. (Note that a route between input material and products produced by input material is termed a branch.)
- 4) The range of the specification of the chips produced from the input wafer and the specification of the packages produced from the input chip are known and fixed over the considered planning horizon.
- 5) The demand for each type of packages in each period is known but may vary period by period.
- 6) Setup and production costs are different for each type of wafers, and chip and package holding costs are fixed.
- 7) Lost sales costs may vary according to demand priorities when the demands are not satisfied.
- 8) No backorder is allowed for unsatisfied demands.
- 9) There is no work-in-process (WIP) or planned in-transit volume at the initial stage of planning.

In the following, we give a mixed integer programming (MIP) formulation for the problem. This formulation is used for a clear description of the problem as well as for finding an optimal solution with a commercial integer programming solver, which will be used as a benchmark solution in computational experiments to be done later in this study.

In the formulation and throughout the paper, we use the following notation.

Indices and parameters

i	index for wafer types ($i = 1, \dots, n$)
j	index for chip types ($j = 1, \dots, m$)
k	index for recipe to produce target package types ($k = 1, \dots, K$)
l	index for produced package types ($l = 1, \dots, L$)
p_{ij}	production ratio of chip type j produced from wafer type i
q_{kl}	production ratio of package type l produced from chips that are input for recipe k
D_l	demand of package type l
M_{wafer}	input wafer capacity, i.e., the maximum number of wafers that can be input into FAB in each period
C^{PI}	package inventory holding cost of one unit
C^{CI}	chip inventory holding cost of one unit
C_i^S	setup cost of wafer type i
C_i^P	production cost of one unit of wafer type i
C_l^U	lost sales cost of one unit of package type l
K_j	set of recipes that use chip type j
J_k	set of chip types that can be used for recipe k

Decision variables

x_i	input quantity of wafer type i
y_j	input quantity of chip type j
h_{jk}	input quantity from chip type j to recipe k
z_k	input quantity of chip for recipe k
u_l	lost sales of package type
I_j^C	inventory level of chip type j , and $I_{j,0}^C$ is initial inventory level of chip type j
I_l^P	inventory level of package type l , and $I_{l,0}^P$ is initial inventory level of package type l
B_i	= 1 if wafer type i is input and 0 otherwise. ($B_{i,0} = 1$ if wafer type i is input in previous period.)
S_i	= 1 if wafer type i is not input in previous period but input in this period (if setup cost is incurred), and 0 otherwise

Now, we present a mixed integer program formulation for the problem.

$$[P] \text{ Minimize } \sum_{i=1}^n (C_i^S S_i + C_i^P x_i) + C^{CI} \sum_{j=1}^m I_j^C + C^{PI} \sum_{l=1}^L I_l^P + \sum_{l=1}^L C_l^U u_l \quad (1)$$

$$\text{subject to } \sum_{i=1}^n x_i \leq M_{wafer} \quad (2)$$

$$I_{j,0}^C + \sum_{i=1}^n p_{ij} x_i - y_j = I_j^C \quad \forall j \quad (3)$$

$$y_j = \sum_{k \in K_j} h_{jk} \quad \forall j \quad (4)$$

$$z_k = \sum_{j \in J_k} h_{jk} \quad \forall k \quad (5)$$

$$I_{l,0}^P + \sum_{k=1}^K q_{kl} z_k + u_l = D_l + I_l^P \quad \forall l \quad (6)$$

$$x_i \leq M_{wafer} B_i \quad \forall i \tag{7}$$

$$x_i \geq B_i \quad \forall i \tag{8}$$

$$S_i \geq B_i - B_{i,0} \quad \forall i \tag{9}$$

$$0 \leq u_l \leq D_l \quad \forall l \tag{10}$$

$$B_i, S_i \in \{0, 1\} \quad \forall i \tag{11}$$

$$x_i, y_j, h_{jk}, I_j^C \geq 0 \text{ and integer} \quad \forall i, j, k \tag{12}$$

$$z_k, u_l, I_l^P \geq 0 \quad \forall k, l \tag{13}$$

The objective function, to be minimized, represents the production-related costs including setup, production, inventory holding, and lost sales costs across the planning horizon. Constraint (2) is a capacity constraint at the FAB. Constraint (3) ensures that the total inventory of each type of chips at the end of period is equal to its inventory in the previous period plus the total production of that chip in that period minus its total consumption in that period. Total quantity of each type of chips produced is calculated as the sum of the quantities yielded by each of the corresponding processes regarding the production ratio (p_{ij}) of each process (FAB). Constraints (4) and (5) represent an allocation of chips to recipe. In other words, the total quantity of chips allocated to the recipe is equal to the total quantity of chips loaded into each recipe. Constraint (6) represents a balance equation, that is, the left-hand side specifies the sum of the package inventory in the previous period, and the production quantity and lost sales of the package in the current period, and the right-hand side specifies the sum of the demand and inventory of the package in the current period. Constraints (7)-(9) represent the relationships of setup and production. In particular, constraint (9) represents the condition under when setup cost occurs. That is, a setup cost is generated when there is a production amount previously and there is no initial production amount. Constraint (10) requires that the lost sales should not be greater than the demand of package. Note that information about the production ratio in FAB and PKG stages used in this study is close to historical data obtained from an LED company. Constraints (11)-(13) are non-negative constraints or integer constrains of the decision variables.

3. Lagrangian Relaxation Approach for Planning Decision. To reduce the computational time to solve the problem [P] exactly, we propose the solution approach based on Lagrangian relaxation and sub-gradient optimization methods. In the algorithm, the problem is relaxed by dualizing a set of constraints with Lagrangian multipliers and then the relaxed problem is decomposed in two subproblems. Here, we show the following relaxed problem, [LR], by relaxing constraint equations (4) with Lagrangian multiplier λ , where λ is a vector with nonnegative elements, i.e., $\lambda_j \geq 0$ for all j .

The original problem [P] is relaxed by dualizing constraint (4) with Lagrangian multipliers, $\lambda_j \geq 0$. The relaxed problem, [LR], is given below. Note that an objective function value of the [LR] is a lower bound on the optimal solution value of [P].

[LR] Minimize

$$\begin{aligned} & \sum_{i=1}^n C_i^S S_i + \sum_{i=1}^n C_i^P x_i + C^{CI} \sum_{j=1}^m I_j^C + C^{PI} \sum_{l=1}^L I_l^P + \sum_{l=1}^L C_l^U u_l \\ & + \sum_{j=1}^m \lambda_j \left(\sum_{k \in K_j} h_{jk} - y_j \right) \end{aligned} \tag{14}$$

subject to (2), (3), (5)-(13) and,

$$\lambda_j \geq 0 \quad \forall j \tag{15}$$

Then, the problem [LR] is decomposed into two subproblems as follows.

[SP1(FAB)]

$$\text{Minimize } \sum_{i=1}^n C_i^S S_i + \sum_{i=1}^n C_i^P x_i + C^{CI} \sum_{j=1}^m I_j^C + \sum_{j=1}^m \lambda_j(-y_j)$$

subject to (5) to (8)

$$\text{subject to } \sum_{i=1}^n x_i \leq M_{wafer} \tag{2}$$

$$I_{j,0}^C + \sum_{i=1}^n p_{ij} x_i - y_j = I_j^C \quad \forall j \tag{3}$$

$$x_i \leq M_{wafer} B_i \quad \forall i \tag{7}$$

$$x_i \geq B_i \quad \forall i \tag{8}$$

$$S_i \geq B_i - B_{i,0} \quad \forall i \tag{9}$$

$$B_i, S_i \in \{0, 1\} \quad \forall i \tag{11}$$

$$x_i, y_j, I_j^C \geq 0 \text{ and integer } \quad \forall i, j, k \tag{12-1}$$

[SP2(PKG)]

$$\text{Minimize } C^{PI} \sum_{l=1}^L I_l^P + \sum_{l=1}^L C_l^U u_l + \sum_{j=1}^m \lambda_j \left(\sum_{k \in K_j} h_{jk} \right)$$

$$\text{subject to } z_k = \sum_{j \in J_k} h_{jk} \quad \forall k \tag{5}$$

$$I_{l,0}^P + \sum_{k=1}^K q_{kl} z_k + u_l = D_l + I_l^P \quad \forall l \tag{6}$$

$$0 \leq u_l \leq D_l \quad \forall l \tag{10}$$

$$h_{jk} \geq 0 \text{ and integer } \quad \forall j, k \tag{12-2}$$

$$z_k, u_l, I_l^P \geq 0 \quad \forall k, l \tag{13}$$

In order to search the best Lagrangian multipliers, the subgradient method is adopted in general. After the multipliers, λ_j , corresponding to mismatch between produced quantity in fabrication and release quantity to package of chip type j , can be obtained by iterative approach. The Lagrangian multiplier at the next iteration, can be calculated as $\lambda_j^{t+1} = \lambda_j^t + \beta^t \left(\sum_{k \in K_j} h_{jk} - y_j \right)$. Here, β^t is a positive gap size calculated as $\beta^t = \rho^t (UB^t - Z(LR(\theta^t))) / \left\| \sum_{k \in K_j} h_{jk} - y_j \right\|^2$, where UB^t is the best upper bound. The best upper bound means the best feasible solution calculated at the former iteration and the value ρ^t , which is positive, is set to 1 at the first iteration, and this number is reduced by a half if the lower bound UB of problem [P], called as LB, is not decreased for a predetermined number of iterations. In this research we set the maximum iteration number as 20 with regarding the computational performance. The overall procedure for solving [P] with Lagrangian relaxation and subgradient method can be summarized as follows. For the stopping conditions, parameters U , ε , and B are used. Each sub problem is solved by iteratively updating of Lagrangian multipliers. The stopping condition of the iteration is that any one of three termination conditions is satisfied.

Stopping conditions for iteration

- 1) The iteration count reaches predetermined limit (defined as U)
- 2) The gap between an upper bound, UB, and a lower bound, LB, becomes less than a predetermined limit (defined as ε)
- 3) The lower bound has not been decreased for a predetermined number of iterations (defined as B)

Procedure 1. (Solving original problem [P])

Step 0 Set $u = 0, b = 0$ and set all decision variables to 0.

Step 1 If $u > U$ or $b > B$, stop; otherwise, go to step 2.

Step 2 Find the optimal solution of [SP1(FAB)] and [SP2(PKG)], and increase the number of u (i.e., $u \leftarrow u + 1$). If the optimal solution of [SP1(FAB)] and [SP2(PKG)] is feasible to [P], the obtained solution is optimal. Terminate the procedure. Otherwise, go to the next step.

Step 3 Find a lower bound, LB, from the solution found in step 2, and update the best lower bound and set $b \leftarrow 0$ if the newly found lower bound is less than current best lower bound. Otherwise, set $b \leftarrow b + 1$ and update Lagrangian multipliers by the subgradient optimization method.

Step 4 Find a feasible solution for [P]. If ratio of difference UB and LB, $(UB - LB)/LB$ is less than ε , terminate. Otherwise, go to step 1.

We prepared computational test sets based on the real production data in an LED manufacturer in Korea. We tested 3 kinds of demand ratio (DR), and 10 replicates for each test data set. Here, the DR is defined as the total demands amount over production capacity.

Results of the computational test are shown in Table 1. The average percentage gap of the total cost of the Lagrangian relaxation heuristics algorithm from optimal solution is obtained by CPLEX than 5%. The CPU times to obtain the optimal solution of problem [P] by CPLEX are over 2 hours in average, while half hours in max CPU time by the proposed Lagrangian relaxation method. Note that, we considered only single period production planning problem for LED manufacturing.

TABLE 1. Performance (percentage gap) of the algorithm

Number of wafer types	DR	PG [†] (%)		
		MIN	AVG	MAX
$n = 15$	0.8	4.17	6.06	8.74
	1.0	2.64	5.76	9.68
	1.2	3.60	5.31	8.95
Sum/Average		5.71		
$n = 20$	0.8	4.16	5.50	7.70
	1.0	3.59	5.72	8.74
	1.2	3.31	5.95	8.65
Sum/Average		5.72		

[†]Percentage gap of the heuristic solution from solutions obtained by CPLEX within 10 h of CPU time.

4. Conclusions. In this paper, we propose Lagrangian relaxation heuristics to obtain near optimal production plan for LED wafer fabrication and chip packaging. In the front-end process of the LED manufacturing, wafers are fabricated with circuit patterning. In this process, product type of wafers is determined by their die sizes, and wave length of emitting light. In the backend process, the wave length can be adjusted by applying a fluorescent substance on the surface of LED dies. The product types are binned according

to the wave length, and this binning is not stabilized and overlapped with different product types of wafer fabrication. Therefore, the production plan, determining release quantity of wafers and chips to production, should be recalculated quickly enough in the case that the binning ratio becomes greatly disturbed to meet the customers' demand.

Results of computational tests showed that the near optimal production plan can be obtained within a half hour, while the optimal solution can be obtained around 2 hours CPU time. The percentage gap between optimal and Lagrangian heuristics is less than 5% for the single period problem. For the further works, we consider the multi-period production planning problem for the two-stage production of LED with random yield to obtain long term production and inventory control plan.

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