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DIGITAL FREQUENCY-LOCKED LOOP WITH LOW FREQUENCY ERROR BASED ON MULTI-PHASE CLOCK

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Abstract. *For the clock generation circuit for clock distribution that drives each system of mobile communication devices, a stable clock supply and quick recovery from a stopped state are desired. In this paper, we propose digital frequency-locked loop (DFLL) with low frequency error based on multi-phase clock. In this circuit, the frequency detection error between the input and output signals can be reduced to one phase difference of the multi-phase clock. In line with this, the steady frequency error of the output signal can also be set to one phase difference of the multi-phase clock. In addition, the characteristics of the pill-in time and the corresponding cycle slip are inherited from the previously proposed circuit.*
Keywords: Frequency-locked loop, Multi-phase clock, Frequency error, Divider, PLL

1. **Introduction.** In an advanced information society, various information devices will become the central content that makes people's social life more comfortable. Among them, mobile communication devices will play an increasingly important role in transferring various information from physical space to cyber space. The microprocessor in that mobile communication device has multiple clock generation circuits for clock distribution to drive other circuits in the system, in addition to the clock generation circuits that drive itself. And, these clocks are used to synchronize the operation of the processor with the external system. Hence, the supply of a stable clock is a crucial factor in determining the accuracy of the entire system [1-3]. Also, in mobile communication devices, the standby state during use is extremely long, so the power consumption in that state greatly affects the power consumption of the entire system from the perspective of battery life. Therefore, if the clock can be stopped during standby and supplied quickly when it is restored, power consumption can be reduced without compromising the accuracy of the system.

A widely used circuit for this clock generation is the phase-locked loop (PLL). However, because PLLs require phase control, they require a certain amount of time to generate a

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stable clock from the system standby state. To improve this, we can set a smaller time constant for the filter in the loop, but this will increase the jitter of the output signal [4].

For this reason, the authors proposed an all-digital frequency-locked loop (DFLL), which does not require phase control and thus allows for quick clock generation [5]. The DFLL was able to complete the initial frequency pull-in in one cycle of the input signal, and was not affected by the cycle slip between the input and output signals. Next, we proposed a DFLL that solves the problem of falling into a pseudo-locked state where the frequencies of the input and output signals are synchronized while keeping a $1 : n$ (n is an integer excluding "1") relationship [6]. However, these proposed DFLLs were configured to use the rising edge of the reference clock to control the loop. Hence, there was an error of less than one cycle of the reference clock in detecting the frequency error between the input and output signals, and this occurred as an error in the output signal. To reduce the error, the authors proposed a DFLL based on a double-edge counter [7]. Since the DFLL was controlled using both the rising and falling edges of the reference clock, the detection error between the input and output signals could be reduced to less than half a cycle of the reference clock.

On the other hand, general conventional digital circuits are configured to control the system by using the rising or falling edge of a single-clock. Even in PLLs and FLLs with a digital configuration, their control was based on one cycle or half cycle of the reference clock. For this reason, the phase error control in PLL and the frequency error control in FLL are also controlled in this unit, so these circuits had a control error of up to one or half a cycle of the reference clock. Therefore, in order to improve the accuracy of the error control of these circuits, it was necessary to improve the control unit. In recent years, there have been research reports on digital circuits using multi-phase clock to improve them [8-10].

In this paper, we propose a DFLL based on multi-phase clock that can obtain output signals with higher frequency accuracy. The proposed DFLL uses a multi-phase clock to control the counters that constitutes the circuit. Therefore, it is possible to control in units of one phase difference of multi-phase clock, and the frequency detection error between the input and output signals can be reduced compared to the conventional system. As a result, the steady frequency error of the output signal is reduced and stable operation is possible. In addition, the characteristics of the pill-in time and the corresponding cycle slip are inherited from the previously proposed circuit.

In the following, Chapter 2 describes the basic operation of the frequency error detection of the conventional DFLL shown in [5,7], and Chapter 3 describes the circuit configuration of the proposed DFLL and its operation analysis. Chapter 4 shows the simulation results using Verilog-HDL. Finally, Chapter 5 presents the conclusion.

2. Frequency Error Detection of Conventional DFLL.

Figure 1 shows a block diagram of a conventional DFLL shown in [5,7]. Figure 2 shows the operational waveforms in its frequency error detection. DFLL is a method that detects the error value by counting the number of reference clocks that pass between the frequency error of the input and output signals (between time t_1 and t_3). Therefore, at the start of error detection, if the edge of the reference clock changes (time t_2) immediately after the frequency error signal is generated (time t_1), the conventional DFLL using the single-clock method will produce a detection error of less than one cycle of the reference clock. On the other hand, the DFLL based on the double edge counter has a detection error of less than half a cycle. In addition, at the end of error detection, if the edge of the reference clock changes (time t_4) immediately after the frequency error signal falls (time t_3), the same detection error as at the start of error detection will occur respectively.

The conventional DFLL is configured to feed back a signal divided by the reference clock based on this detection value as the output signal. Therefore, the detection error of

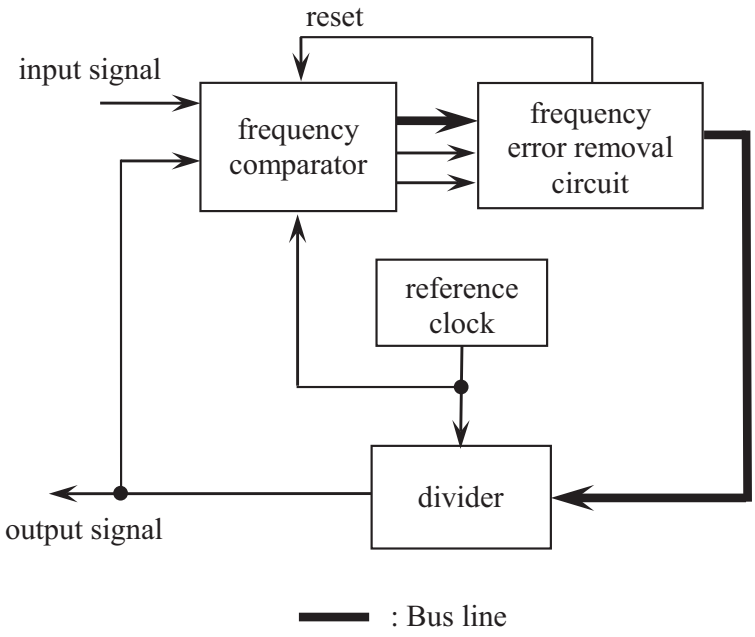

FIGURE 1. Block diagram of the conventional DFLL

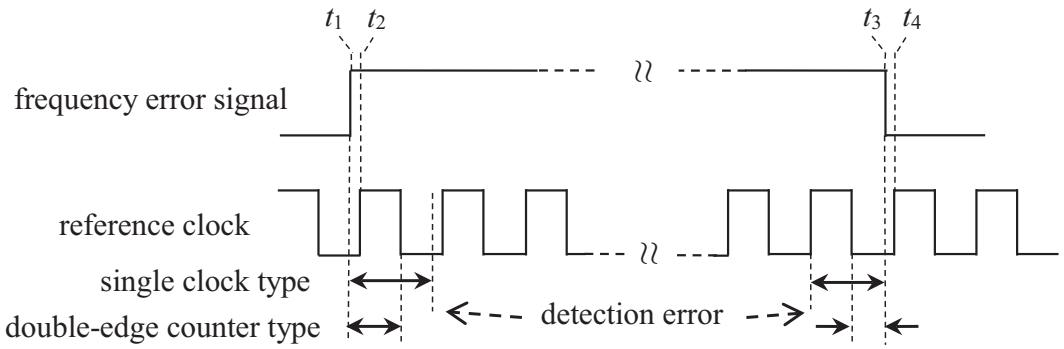

FIGURE 2. Waveforms for frequency error detection of the conventional DFLL

the frequency error will be directly generated as the frequency error of the output signal. As a result, the steady frequency error of the output signal occurs less than one cycle of the reference clock in the conventional DFLL using the single-clock method, and less than half a cycle in the double-edge counter method.

3. Configuration and Operational Analysis of the Proposed DFLL.

3.1. Circuit configuration of the proposed DFLL. Figure 3 shows the circuit configuration of the proposed DFLL. Figure 4 shows the waveform of the multi-phase clock used in the proposed DFLL. The multi-phase clocks should be set so that the phase difference between each clock is a fixed interval. Here, T-FF1, T-FF2, T-FF3, EX-OR, logic gate, and U/D-counter_1$\sim k$ shown in Figure 3 constitute the digital frequency comparator. The U/D-counter_1$\sim k$ are controlled up/down by signals from the logic gate, and only one of the multi-phase clock $\text{clk}_{1\sim k}$ are used as the count clock. The FEC is a control circuit for removing frequency errors between the input and output signals. $1+1/k$ is a $1+1/k$ divider that divides the multi-phase clock by shifting it by one phase as shown in Figure 5. The DC compares the value "n" of the counter that counts the clock to be supplied to the divider with the number "m" to be divided by $1+1/k$ from the FEC. While the relationship is "$n \leq m$", the $1+1/k$ divider supplies the divider with a signal

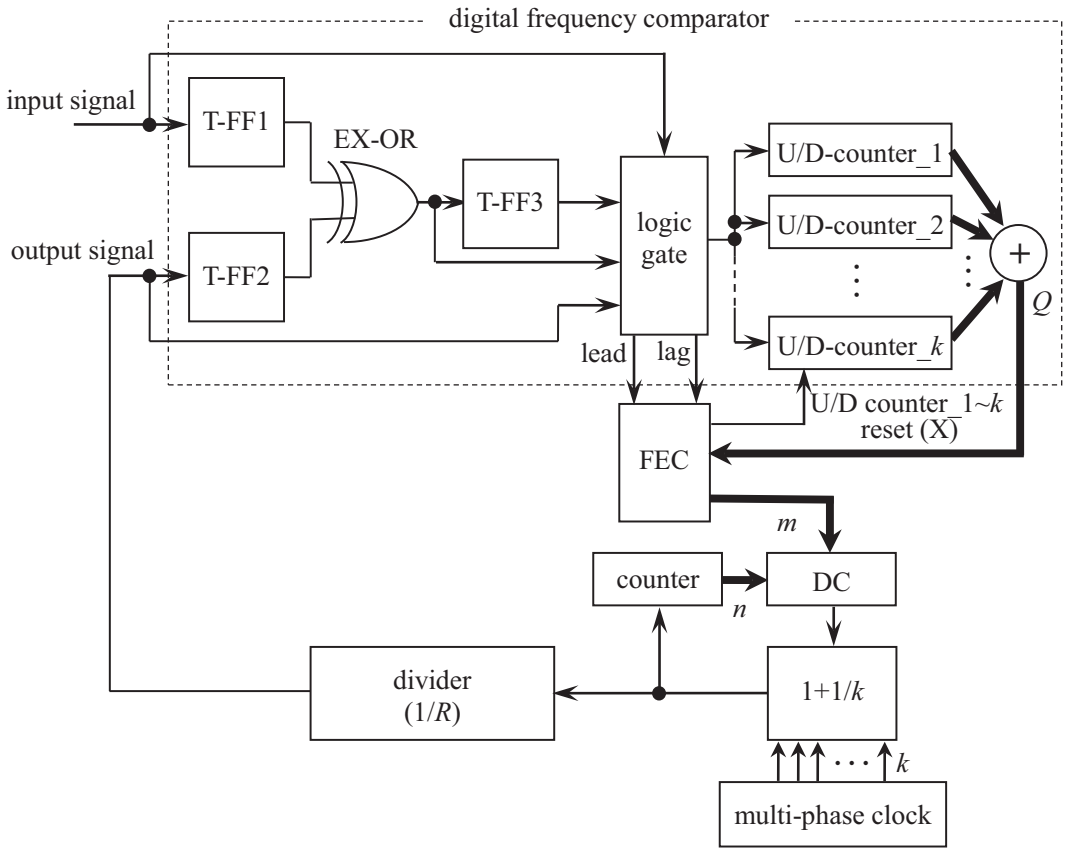

FIGURE 3. Circuit configuration of the proposed DFLL based on multi-phase clock

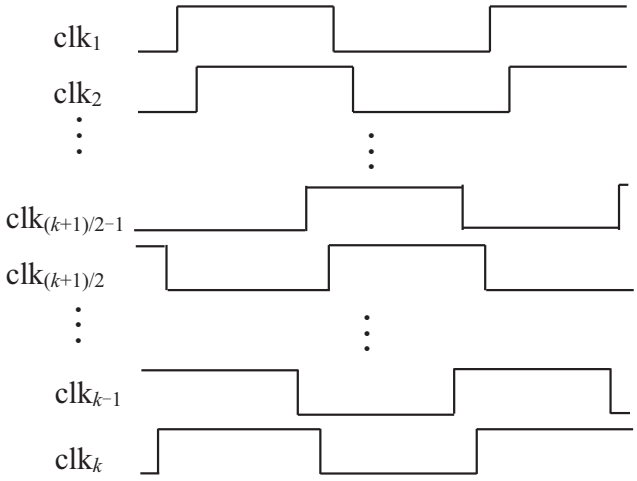

FIGURE 4. Timing chart of multi-phase clock

that is a multi-phase clock divided by $1+1/k$. While "$n > m$", the $1+1/k$ division is stopped, and when "$n = m$", the selected multi-phase clock is directly supplied to the divider.

3.2. **Operational analysis of the proposed DFLL.** Figure 6 shows the operating waveforms of the frequency comparator in the proposed DFLL. When the input signal rises at time t_1, the EX-OR shown in Figure 3 outputs a high level. Next, when the

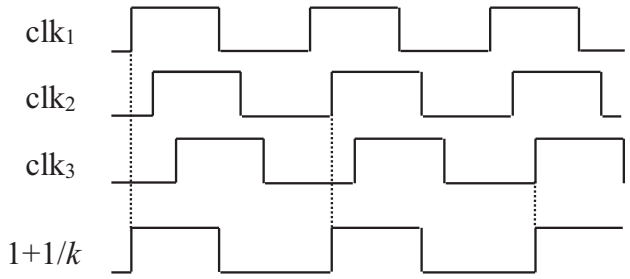

FIGURE 5. Waveforms of $1+1/k$ divider

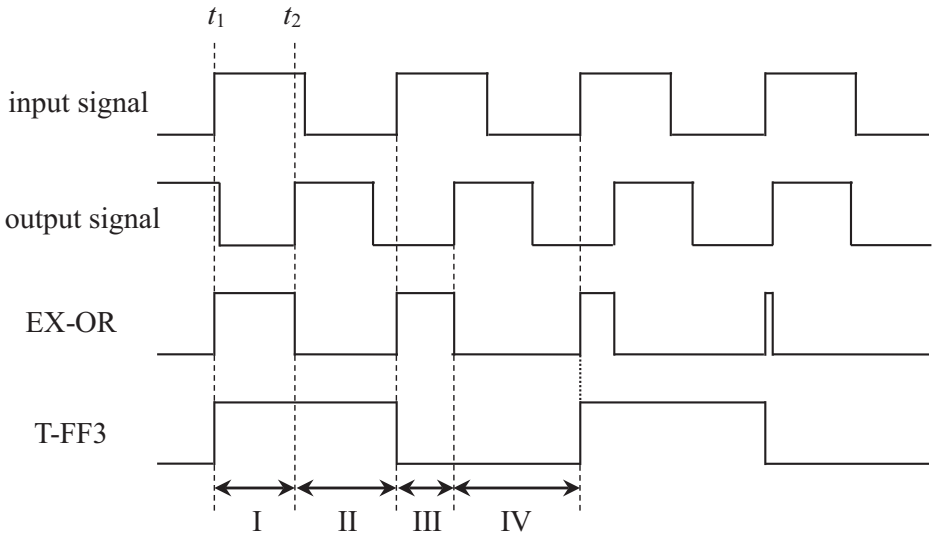

FIGURE 6. Waveforms of frequency comparator

output signal rises at time t_2, and the EX-OR outputs a low level. T-FF3 divides the output from this EX-OR.

Next, we will explain the frequency error detection operation. Now, in state I of Figire 6, U/D counter_1$\sim k$ up-count the number of each multi-phase clock that passes through while the output of EX-OR is high, respectively. When the total number of multi-phase clocks (up-count value) that pass through during state I is "Y" and the initial values of U/D counter_1$\sim k$ are "X", the value "Q" of the adder circuit at the end of state I is "$Q = X + Y$".

In state II, the values of U/D counter_1$\sim k$ and the count value "Q" of the addition circuit are held, respectively.

In state III, U/D counter_1$\sim k$ down-count the number of each multi-phase clock that passes through while the output of EX-OR is high, respectively. When the total number (down-count value) of each multi-phase clock that passes during state III is "Z", the value "Q" of the adder circuit is "$Q = X + Y - Z$". As a result, the value "Q" of the adder circuit at the end of state III will be the value corresponding to the frequency error between the input and output signals.

In state IV, the value "Q" of the adder circuit is transferred to the FEC of the next stage. The FEC outputs a new comparison value "m" for DC from the up-count value "Y" and down-count value "Z". Table 1 shows how "m" is calculated according to the phase state between the input and output signals. Also, at this point, the count values of U/D counte_1$\sim k$ are reset to the initial value "X".

TABLE 1. Controll state of dividing ratio according to the phase lead or lag

	State I	State III	$Y > Z$	$Y < Z$
Pattern 1	lead	lead	$m-(Y-Z)$	$m+(Z-Y)$
Pattern 2	lead	lag	$m+(Y-Z)$	$m+(Z-Y)$
Pattern 3	lag	lead	$m-(Y-Z)$	$m-(Z-Y)$
Pattern 4	lag	lag	$m+(Y-Z)$	$m-(Z-Y)$

Next, let us consider the frequency of the output signal determined by the above control. Figure 7 shows the control waveform of the output signal of the proposed DFLL. The output signal is obtained by dividing the clock from the 1+1/k divider by the divider (division ratio "R"). Therefore, one cycle of the output signal is composed of "m" clocks that divide the multi-phase clock by 1+1/k and "$R-m$" clocks that do not.

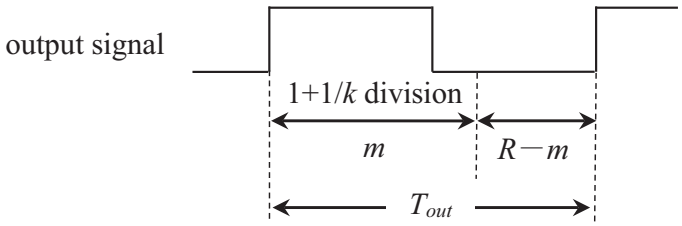

FIGURE 7. Output signal control

Here, when the time of one cycle of the multi-phase clock is t_{mp}, the time T_{out} of one cycle of the output signal is

$$T_{out} = m \cdot t_{mp}\left(1+\frac{1}{k}\right) + (R-m)t_{mp} = t_{mp}\left(\frac{m}{k}+R\right) \tag{1}$$

Therefore, the frequency f_{out} of the output signal can be expressed by the following equation.

$$f_{out} = \frac{1}{t_{mp}\left(\frac{m}{k}+R\right)} \tag{2}$$

From the above, the frequency of the output signal of the proposed DFLL will be controlled by one phase difference unit of the multi-phase clock according to the difference between "Y" and "Z".

Next, let us consider the frequency lock-in range of the proposed DFLL. The proposed DFLL is a configuration in which the frequency of the output signal is determined by dividing the clock from the 1+1/k divider by the division ratio "R". Hence, the lock-in range of frequency is determined by "m" and "R". Since the maximum value of "m" is "R", the lower limit of the division ratio "$R_{\min}$" is "$R_{\min} = R$" and the upper limit "$R_{\max}$" is "$R_{\max} = R + (1+1/k)$". Therefore, the frequency lock-in range of the proposed DFLL can be expressed by the following equation

$$\frac{f_{mp}}{R\left(1+\frac{1}{k}\right)} \le f_{in} \le \frac{f_{mp}}{R} \tag{3}$$

where f_{in} is the frequency of the input signal and f_{mp} is the frequency of the multi-phase clock.

Next, let us consider the steady frequency error. In the proposed DFLL, the multi-phase clock and the input signal are not locked. Also, the frequency of the output signal is controlled by dividing the multi-phase clock by 1+1/k. Therefore, since the control is in units of one phase difference of the multi-phase clock, the output signal will have a steady-state frequency error of at most one phase difference of the multi-phase clock.

Hence, since its control is one phase difference unit of the multi-phase clock, the output signal will have a similar steady frequency error. Therefore, the average frequency f_{avg} of the output signal is

$$f_{avg} = \frac{\frac{f_{mp}}{\left(R+\frac{m}{k}\right)} + \frac{f_{mp}}{\left(R+\frac{m}{k}\right)\pm\frac{1}{k}}}{2} \tag{4}$$

From the above, if the dividing ratio R is set somewhat large, the effect of this error on the jitter suppression effect can be ignored.

4. **Simulation Result.** We used Verilog-HDL, a hardware description language, for our simulations.

Figure 8 shows the simulated waveforms of various parts of the conventional DFLL. In the conventional DFLL, depending on the timing with the reference clock, counting operation immediately after the rising edge of the frequency error signal or uncounted operation immediately after the falling edge occurs. From this, it is found that the conventional single-clock method produces a detection error of less than one cycle of the reference clock at most, and the double-edge counter method produces a detection error of less than half a cycle.

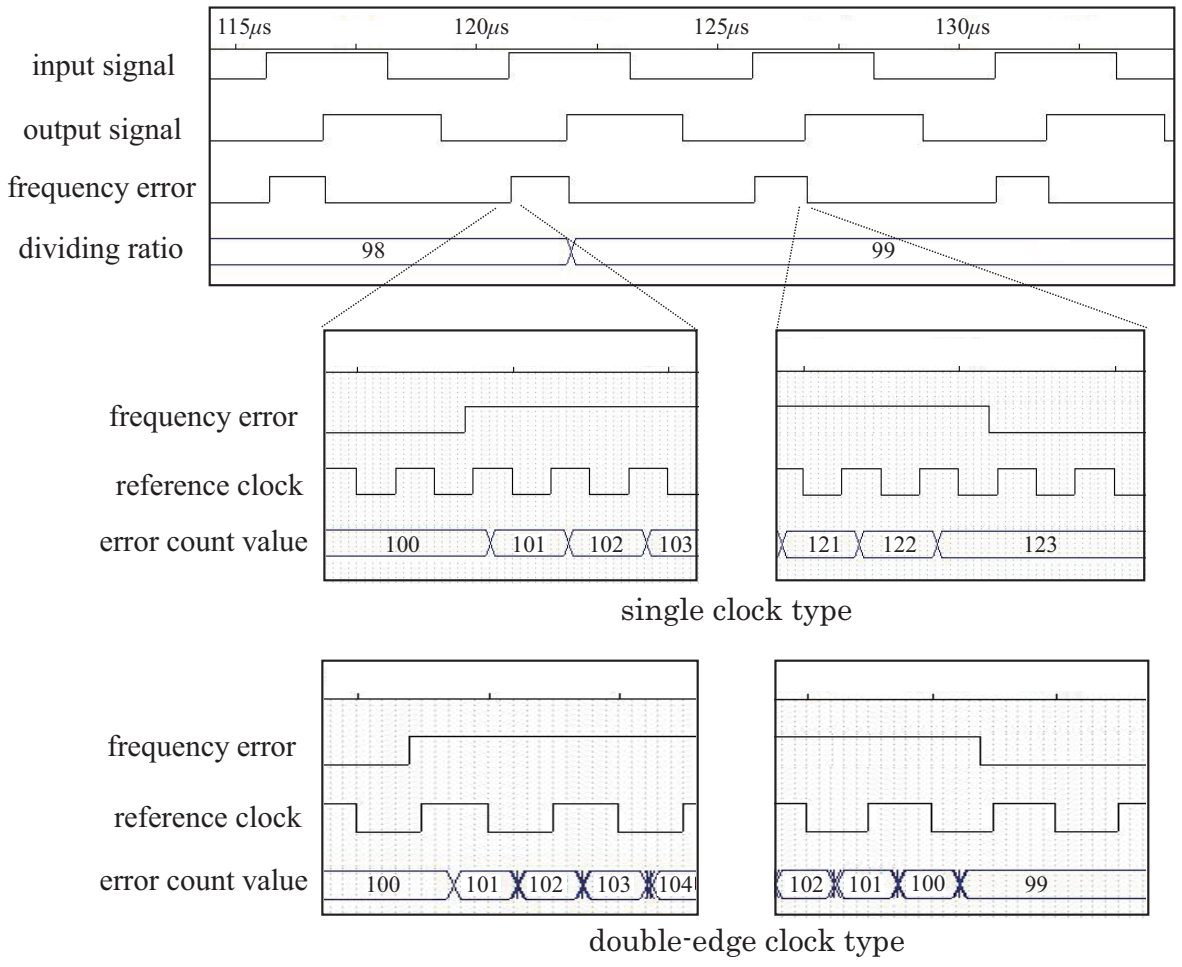

FIGURE 8. Simulation waveforms of the conventional DFLL

Figure 9 shows the simulated waveforms of each part of the proposed DFLL when the number of phases of the multi-phase clock is set to $k = 7$ and the division ratio of divider is set to $R = 100$. In the proposed DFLL, the count error after the frequency error signal rises or falls is within one phase difference of the multi-phase clock. From this, it is found

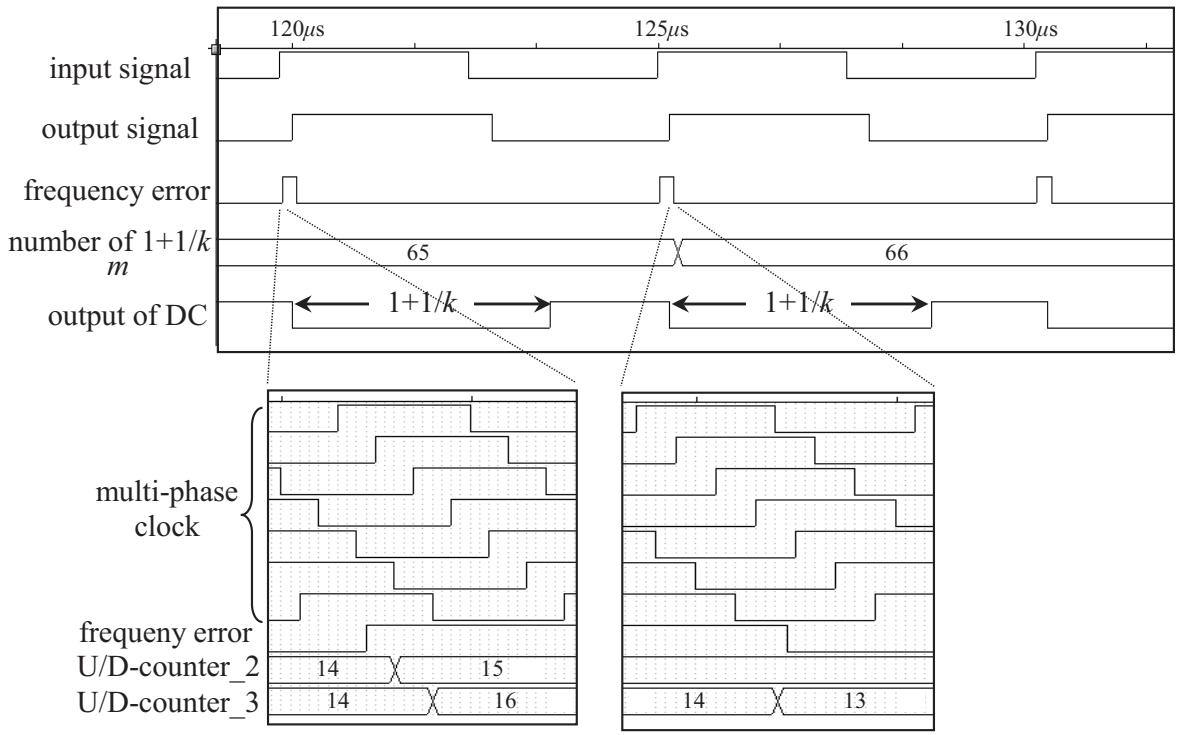

FIGURE 9. Simulation waveforms of the proposed DFLL

that the detection error can be reduced to $1/k$ compared to the conventional single-clock method and about $1/(2k)$ compared to the double edge counter method.

In addition, in the proposed DFLL, when $R = 100$, $k = 7$, and $f_{mp} = 2$ MHz, the synchronization range is 17.5 kHz to 20.0 kHz, and the steady-state frequency error is within one phase difference of the multiphase clock, which satisfies Equations (3) and (4).

5. **Conclusion.** In this paper, we proposed the DFLL that can be controlled by one phase difference unit of multi-phase clock. This circuit was able to reduce the frequency detection error and steady frequency error between the input and output signals to $1/k$ compared to the conventional single-clock method and about $1/(2k)$ compared to the double-edge counter method. Also, it was confirmed that the pull-in time and cycle slip response inherited the characteristics of the conventional DFLL.

In the future, we plan to further verify the characteristics and study its practicality.

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