CAPACITANCES DESIGN METHOD OF THE MAIN NEURON CMOS INVERTER OF A 4-INPUT VARIABLE LOGIC CIRCUIT WITH FG CALIBRATION

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ABSTRACT. *A 4-input Variable Logic Circuit with FGC (VLC) is expected as a logic element of Field Programmable Gate Array (FPGA), but the detailed design method has not been described in conventional papers. In this paper, we describe the process of the main νCMOS design method. It is proved that the capacitances of the control gates and the capacitances of the input gates are equal and how to obtain the capacitances of each middle gate.*
Keywords: Neuron MOS transistor, Neuron CMOS inverter, Variable Logic Circuit, FPGA

1. **Introduction.** FPGA is composed of logic elements, input/output elements, and wiring elements and this time, we focused on logic elements. A 4-input Look-Up Table (LUT) or a 6-input LUT is generally used for this logical element. However, this LUT has problems such as a large circuit area. Therefore, we focused on neuron MOS transistors (νMOS). A νMOS calculates the weighted sum of multiple input voltages and performs the threshold operation based on the weighted sum [1-4]. We proposed a 4-input Variable Logic Circuit with FGC (VLC) (Figure 1) to develop a new FPGA using neuron Complementary Metal Oxide Semiconductor inverter (νCMOS) that used νMOS [5-8]. VLC realizes eight logical functions, i.e., AND, NAND, OR, NOR, XNOR, XOR, identity "1" and identity "0" by changing the three control signals. In the conventional paper, the explanation of the VLC was explained by Floating-Gate Potential Diagram (FPD) based on the ratio of the capacitances prepared in advance. However, the detailed design method for the ratio of the capacitances was not described. In this paper, we build the design theory of the main νCMOS (νCMOS$_\mathrm{M}$). We prove that the capacitances of the control gates and the capacitances of the input gates are equal and how to obtain the capacitances of each middle gates. After that, we will illustrate the FPD based on each capacitance ratio of the three νCMOS and explain the detailed operation of the proposed circuit. In addition, we will verify their operation by HSPICE simulation.

This paper consists of 5 chapters. First, Chapter 1 is an introduction and describes the research background, research purpose, and structure of this paper. Next, Chapter 2 describes the circuit configuration of the conventional circuit. Chapter 3 describes the νCMOS$_\mathrm{M}$ design method. Chapter 4 describes the simulation conditions and simulation result. Finally, Chapter 5 is a conclusion and summarizes the results obtained in this study. Furthermore, the remaining issues are described.
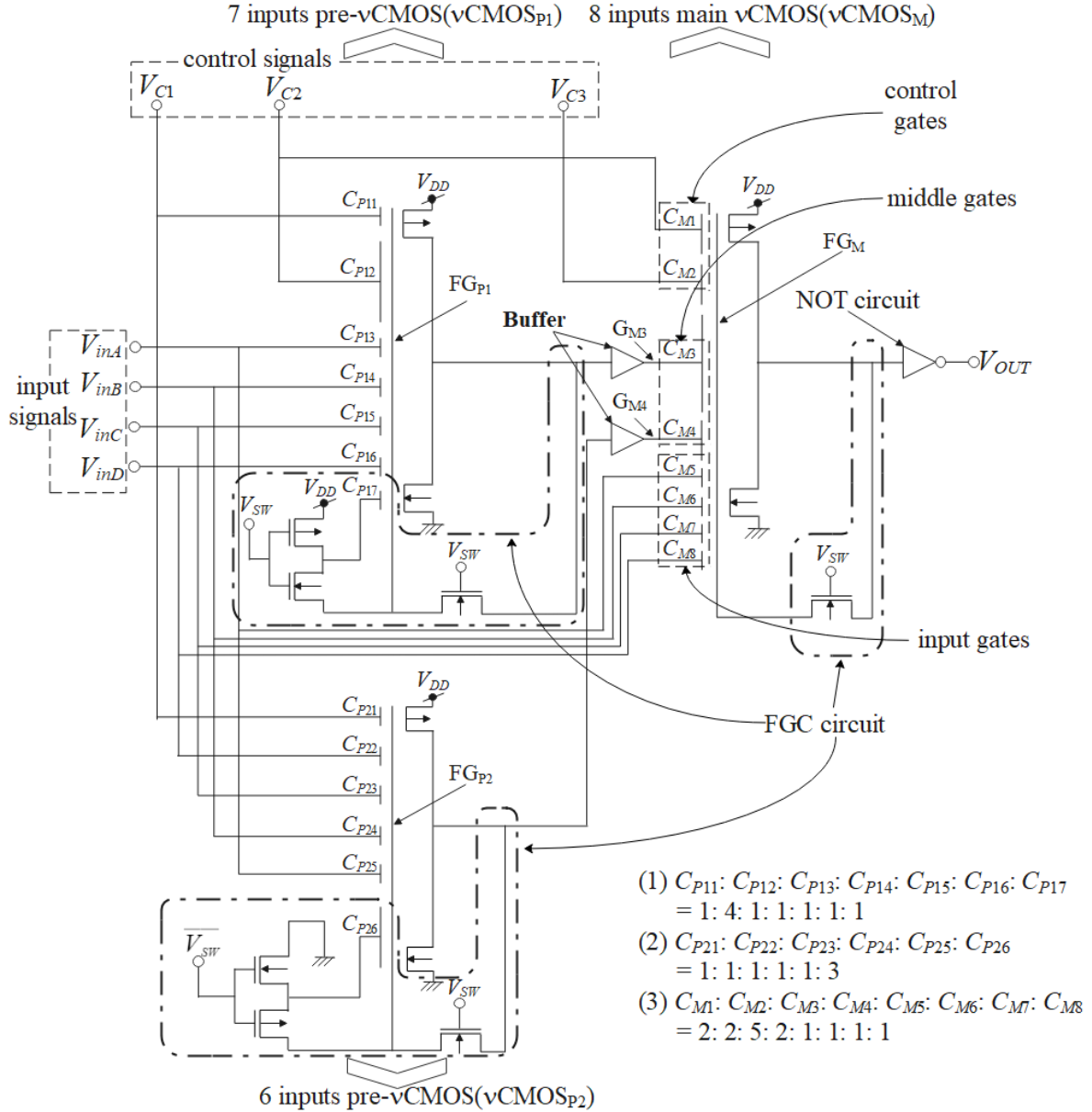
7 inputs pre-νCMOS(νCMOS$_{P1}$)   8 inputs main νCMOS(νCMOS$_M$)

control signals

V_{C1} V_{C2} V_{C3}

control gates

middle gates

FG$_M$

NOT circuit

V_{DD} C_{P11}

C_{P12} FG$_{P1}$

C_{P13} Buffer   G$_{M3}$

C_{P14}

C_{P15} G$_{M4}$

C_{P16}

V_{DD} C_{P17}

V_{SW}

V_{SW}

C_{M1}

C_{M2}

C_{M3}

C_{M4}

C_{M5}

C_{M6}

C_{M7}

C_{M8}

V_{SW}

V_{OUT}

input gates

FGC circuit

input signals V_{inA} V_{inB} V_{inC} V_{inD}

V_{DD}

C_{P21}

C_{P22}

C_{P23} FG$_{P2}$

C_{P24}

C_{P25}

$\overline{V_{SW}}$ C_{P26}

V_{SW} V_{SW}

6 inputs pre-νCMOS(νCMOS$_{P2}$)

(1) C_{P11}: C_{P12}: C_{P13}: C_{P14}: C_{P15}: C_{P16}: C_{P17}
= 1: 4: 1: 1: 1: 1: 1
(2) C_{P21}: C_{P22}: C_{P23}: C_{P24}: C_{P25}: C_{P26}
= 1: 1: 1: 1: 1: 3
(3) C_{M1}: C_{M2}: C_{M3}: C_{M4}: C_{M5}: C_{M6}: C_{M7}: C_{M8}
= 2: 2: 5: 2: 1: 1: 1: 1

FIGURE 1. 4-input variable logic circuit with FGC

2. Conventional Circuit.

2.1. **Circuit configuration.** The basic configuration consists of two pre-νCMOS (νCMOS$_{P1}$, νCMOS$_{P2}$) with an FGC circuit and one νCMOS$_M$. This circuit realizes a 4-input symmetric logic function (① to ⑧ in Table 1) including XOR and XNOR by generating a two-step threshold operation with two pre-νCMOS. As a basic operation, FGC operation (operation to stabilize Floating-Gate) [1] is performed with the switch signal V_{SW}. After that, when the three control signals (V_{C1}, V_{C2}, V_{C3}) are changed, one of the eight types of logic functions is obtained as the output signal V_{OUT} along with the change of the four input signals (V_{inA}, V_{inB}, V_{inC}, V_{inD}). In the conventional circuit of Figure 1, νCMOS$_{P1}$, νCMOS$_{P2}$ and νCMOS$_M$ are 7-input, 6-input and 8-input νCMOS, FG$_{P1}$, FG$_{P2}$ and FG$_M$ are FG terminals of each νCMOS, and G$_{M3}$ and G$_{M4}$ are each input gate terminal, C_{P11} to C_{P17} are the gate capacitances of νCMOS$_{P1}$, C_{P21} to C_{P26} are the gate capacitances of νCMOS$_{P2}$, and C_{M1} to C_{M8} are the gate capacitances of νCMOS$_M$. C_{M1} and C_{M2} are the capacitances that received the output from the control signals (the capacitances of the control gates). C_{M3} and C_{M4} are the capacitances that

TABLE 1. Signal table during FGC operation and variable logic operation

FGC operation (V_{SW} = "1")								Variable logic operation (V_{SW} = "0")			
Control signal			Input signal					Control signal			Logic function
V_{C1}	V_{C2}	V_{C3}	V_{inA}	V_{inB}	V_{inC}	V_{inD}		V_{C1}	V_{C2}	V_{C3}	
								0	0	0	① OR
								0	0	1	② Identity "1"
							$\rightarrow$	0	1	0	③ NOR
								0	1	1	④ XNOR
1	1	1	0	0	0	0		1	0	0	⑤ XOR
								1	0	1	⑥ NAND
								1	1	0	⑦ Identity "0"
								1	1	1	⑧ AND

received the output from the νCMOS$_{P1}$ and νCMOS$_{P2}$ (the capacitances of each middle gate). C_{M5}, C_{M6}, C_{M7} and C_{M8} are the capacitances which received the output from the input signals (the capacitances of the input gates). The capacitances ratio of νCMOS$_{P1}$ is $C_{P11} : C_{P12} : C_{P13} : C_{P14} : C_{P15} : C_{P16} : C_{P17} = 1 : 4 : 1 : 1 : 1 : 1 : 1$. The capacitances ratio of νCMOS$_{P2}$ is $C_{P21} : C_{P22} : C_{P23} : C_{P24} : C_{P25} : C_{P26} = 1 : 1 : 1 : 1 : 1 : 3$. The capacitances ratio of νCMOS$_{M}$ is $C_{M1} : C_{M2} : C_{M3} : C_{M4} : C_{M5} : C_{M6} : C_{M7} : C_{M8} = 2 : 2 : 5 : 2 : 1 : 1 : 1 : 1$. The binary number "0" is 0 [V], "1" is V_{DD} [V], and the inversion threshold voltage of each νCMOS is $V_{DD}/2$.

2.2. **Operation of the circuit.** As shown in Table 1, the operation of the conventional circuit has two stages: FGC operation, and variable logic operation. In FGC operation, the control signal and input signal are set as shown on the left side of Table 1, and when V_{SW} is set to "1", the influence of the electric charge stored in FG is eliminated. In variable logic operation, V_{SW} is set to "0". The behavior of νCMOS$_{M}$ at this time is shown in Figure 2 in FPD. In Figure 2, the horizontal line V_i is given by $(V_{inA}+V_{inB}+V_{inC}+V_{inD})/15$ and is expressed based on the number of "1". The vertical line $V(\text{FG}_M)$ is the potential of FG$_M$. When all the input gate voltages of νCMOS$_{M}$ are "1", $V(\text{FG}_M)$ is the highest value (upper limit of the vertical line), and when all the input gate voltages are "0", $V(\text{FG}_M)$ is the lowest value (lower limit of the vertical line). C_T is the total combined capacitance of νCMOS$_{M}$, $C_T = C_{M1} + C_{M2} + \cdots + C_{M8}$. In the conventional circuit, we set $C_{M5} = C_{M6} = C_{M7} = C_{M8}$ to handle symmetric functions. The Baseline in Figure 2 shows the characteristics of $V(\text{FG}_M)$ concerning V_i when V_{C2}, V_{C3}, $V(\text{G}_{M3})$ and $V(\text{G}_{M4})$ are all "0". When the $V(\text{FG}_M)$ value (thick line) exceeds $V_{DD}/2$ (dashed line), the output voltage V_{OUT} of the conventional circuit is "1". When the $V(\text{FG}_M)$ value (thick line) falls below $V_{DD}/2$ (dashed line), V_{OUT} becomes "0".

Here, it is illustrated that XNOR can be realized by generating a two-step threshold operation from capacitances ratio of (1), (2), and (3) in Figure 1. If the unit capacitance is C, $C_{M5} = C_{M6} = C_{M7} = C_{M8} = $ C/15, and the maximum value (right end) of Baseline in Figure 2 is $4V_{DD}/15$. Next, when V_{C2} and V_{C3} are "1", the Baseline rises by the value of C_{M1} and C_{M2} ($4V_{DD}/15$). V_{INVP1} and V_{INVP2} are the apparent inversion threshold voltages seen from V_i of νCMOS$_{P1}$ and νCMOS$_{P2}$ designed to be $0.5V_{DD}/15$ and $2.5V_{DD}/15$. Then, a thick line in Figure 2 can be drawn based on these two thresholds and the slope of the Baseline. This is the realization of the XNOR function. By changing the control signal, seven types of logical functions other than XNOR can be realized in the same way.

3. **Design of Capacitances of the νCMOS$_{M}$.**

3.1. **Capacitances of C_{M1}, C_{M2}, C_{M5}, C_{M6}, C_{M7} and C_{M8}.** Next, we explain the design method of capacitances of νCMOS$_{M}$. First, we explain why the capacitance of

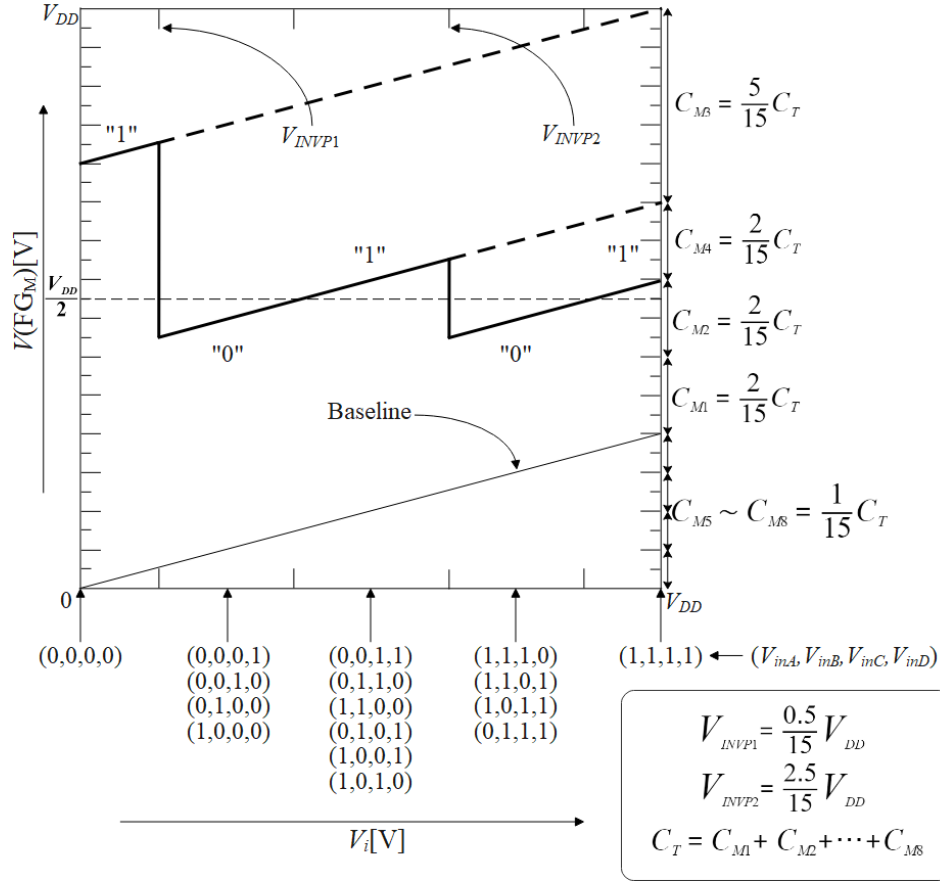FIGURE 2. Realization of each logical function by FPD (XNOR)

TABLE 2. Prerequisites for FGC operation

Prerequisites for FGC operation
1. The output of νCMOS in all stages becomes $V_{DD}/2$
2. All control signals are "1"
3. All input signals are "0"

the input gates and the capacitances of the control gates are equal. The prerequisites for FGC operation are important to explain this reason. Table 2 shows the prerequisites for FGC operation.

Further, as described above, when the minimum value of $V(\mathrm{FG_M})$ is 0, it can be expressed as Equation (1). The maximum value of $V(\mathrm{FG_M})$ is V_{DD}, it can be expressed as Equation (2). $V_{\min}$ is the minimum value of $V(\mathrm{FG_M})$, $V_{\max}$ is the maximum value of $V(\mathrm{FG_M})$. From Equations (1) and (2), it is seen that when $V_{\min}$ is 0 and $V_{\max}$ is V_{DD}, the capacitances of the input signals and the capacitance of the control signals are equal.

$$
\begin{aligned}
V_{\min} &= \frac{1}{2}V_{DD} - \frac{C_{M1}}{C_T}V_{DD} - \frac{C_{M2}}{C_T}V_{DD} - \frac{C_{M3}}{2C_T}V_{DD} - \frac{C_{M4}}{2C_T}V_{DD} \\
&= \frac{1}{2C_T}\left(C_T - 2C_{M1} - 2C_{M2} - C_{M3} - C_{M4}\right)V_{DD} \\
&= \frac{1}{2C_T}\left(C_{M5} + C_{M6} + C_{M7} + C_{M8} - C_{M1} - C_{M2}\right)V_{DD}
\end{aligned}
\tag{1}
$$

$$
V_{\max} = \frac{1}{2}V_{DD} + \frac{C_{M5}}{C_T}V_{DD} + \frac{C_{M6}}{C_T}V_{DD} + \frac{C_{M7}}{C_T}V_{DD} + \frac{C_{M8}}{C_T}V_{DD} + \frac{C_{M3}}{2C_T}V_{DD} + \frac{C_{M4}}{2C_T}V_{DD}
$$

$$= \frac{1}{2C_T} \left(3C_{M5} + 3C_{M6} + 3C_{M7} + 3C_{M8} + C_{M1} + C_{M2} + 2C_{M3} + 2C_{M4} \right) V_{DD}$$

$$= \frac{1}{2C_T} \left(2C_{M5} + 2C_{M6} + 2C_{M7} + 2C_{M8} + 2C_{M1} + 2C_{M2} + 2C_{M3} + 2C_{M4} \right) V_{DD}$$

$$+ \frac{1}{2C_T} \left(C_{M5} + C_{M6} + C_{M7} + C_{M8} - C_{M1} - C_{M2} \right) V_{DD}$$

$$= V_{DD} + \frac{1}{2C_T} \left(C_{M5} + C_{M6} + C_{M7} + C_{M8} - C_{M1} - C_{M2} \right) V_{DD} \tag{2}$$

$$C_T = C_{M1} + C_{M2} + C_{M3} + C_{M4} + C_{M5} + C_{M6} + C_{M7} + C_{M8}$$

3.2. **The capacitances of each middle gate.** Next, we explain how to determine the capacitances of each middle gate. We know that the capacitances of the input gates and the capacitances of the control gates are equal to Equations (1) and (2). So, it can be expressed as Equation (3).

$$C_{M1} + C_{M2} = C_{M5} + C_{M6} + C_{M7} + C_{M8} \tag{3}$$

At this time, the capacitances of the input gates are defined as the unit capacity C. It can be expressed as in Equation (4).

$$C_{M1} + C_{M2} = 4\text{C} \tag{4}$$

Furthermore, since we want to determine V_{OUT} only by the amount of change in the output from the νCMOS$_{P1}$ and νCMOS$_{P2}$, we make the capacitances of the two control signals equal. It can be expressed as in Equations (5) and (6).

$$C_{M1} = 2\text{C} \tag{5}$$

$$C_{M2} = 2\text{C} \tag{6}$$

Next, we consider the capacitances of the middle gates. Consider the conditions that satisfy the logical function XNOR. XNOR becomes "1" only when the number of input signals "1" standing is an even number. Further, since both control signals are "1" at this time, they can be expressed as Equations (7)-(11).

$$\frac{C_{M3} + C_{M4} + 4\text{C}}{C_{M3} + C_{M4} + 8\text{C}} > \frac{1}{2} \tag{7}$$

$$\frac{C_{M4} + 5\text{C}}{C_{M3} + C_{M4} + 8\text{C}} < \frac{1}{2} \tag{8}$$

$$\frac{C_{M4} + 6\text{C}}{C_{M3} + C_{M4} + 8\text{C}} > \frac{1}{2} \tag{9}$$

$$\frac{7\text{C}}{C_{M3} + C_{M4} + 8\text{C}} < \frac{1}{2} \tag{10}$$

$$\frac{8\text{C}}{C_{M3} + C_{M4} + 8\text{C}} > \frac{1}{2} \tag{11}$$

C_{M3} and C_{M4} are designed to move in the order of $(1, 1)$, $(0, 1)$, $(0, 0)$. This is related to the transfer characteristics of skewed inverters. A circuit diagram and a simulation result showing an example of the transfer characteristics of the inverters are shown in Figures 3 and 4 [9].

When Equations (7)-(11) are calculated, they can be expressed as Equations (12)-(16).

$$C_{M3} + C_{M4} > 0 \tag{12}$$

$$C_{M3} - C_{M4} > 2\text{C} \tag{13}$$

$$C_{M3} - C_{M4} < 4\text{C} \tag{14}$$

$$C_{M3} + C_{M4} > 6\text{C} \tag{15}$$

$$C_{M3} + C_{M4} < 8C \tag{16}$$

When Equations (13) and (14) are calculated, it can be expressed as Equation (17).

$$C_{M3} - C_{M4} = 3C \tag{17}$$

When Equations (15) and (16) are calculated, it can be expressed as Equation (18).

$$C_{M3} + C_{M4} = 7C \tag{18}$$

When Equations (17) and (18) are calculated, it can be expressed as Equations (19) and (20). And it can be seen from Equation (12) that Equations (19) and (20) are correct.

$$C_{M3} = 5C \tag{19}$$

$$C_{M4} = 2C \tag{20}$$

From the above, the capacitances of the νCMOS_M are as shown in Figure 1.
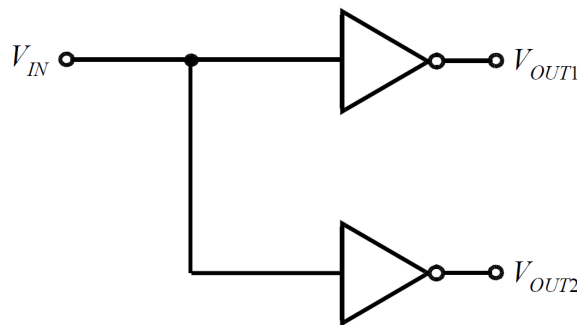
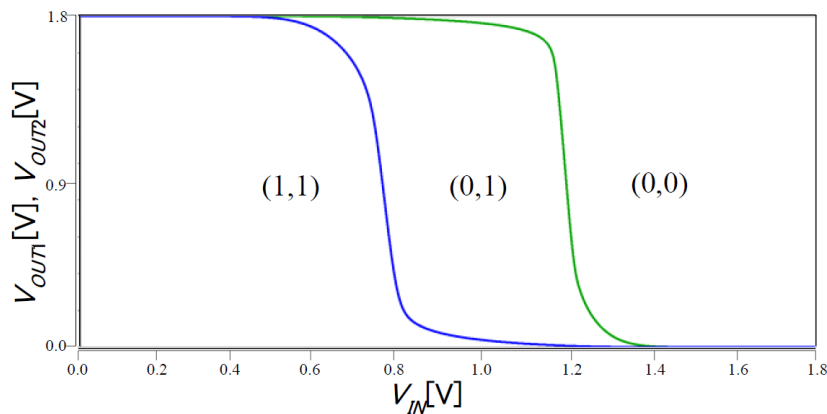FIGURE 3. Example of the transfer characteristics of skewed inverters (circuit diagram)

FIGURE 4. Example of the transfer characteristics of skewed inverters (simulation result)

4. **Operation Result.** The VLC was HSPICE simulated with the device parameters in Table 3. Figure 5 shows the HSPICE simulation results of the VLC. V_{C1}, V_{C2} and V_{C3} are the control signals, and they are input in the order of the values described in Variable Logic Operation in Figure 1. V_{inA}, V_{inB}, V_{inC}, V_{inD} are the input signals. In ④, when $(V_{inA}, V_{inB}, V_{inC}, V_{inD}) = (\text{“0”}, \text{“0”}, \text{“0”}, \text{“0”})$, $V_{OUT} = \text{“1”}$, $(\text{“1”}, \text{“0”}, \text{“0”}, \text{“0”})$, $V_{OUT} = \text{“0”}$, $(\text{“1”}, \text{“1”}, \text{“0”}, \text{“0”})$, $V_{OUT} = \text{“1”}$, $(\text{“1”}, \text{“1”}, \text{“1”}, \text{“0”})$, $V_{OUT} = \text{“0”}$, $(\text{“1”}, \text{“1”}, \text{“1”}, \text{“1”})$, $V_{OUT} = \text{“1”}$. We can confirm the same operation as in Figure 2. This is nothing more than the realization of XNOR function. Similarly, ① to ⑧ in Table 1 can represent any logic functions, that is, AND, OR, NAND, NOR, XOR, XNOR, Identity “1”, Identity “0”.

TABLE 3. Device parameters and simulation conditions

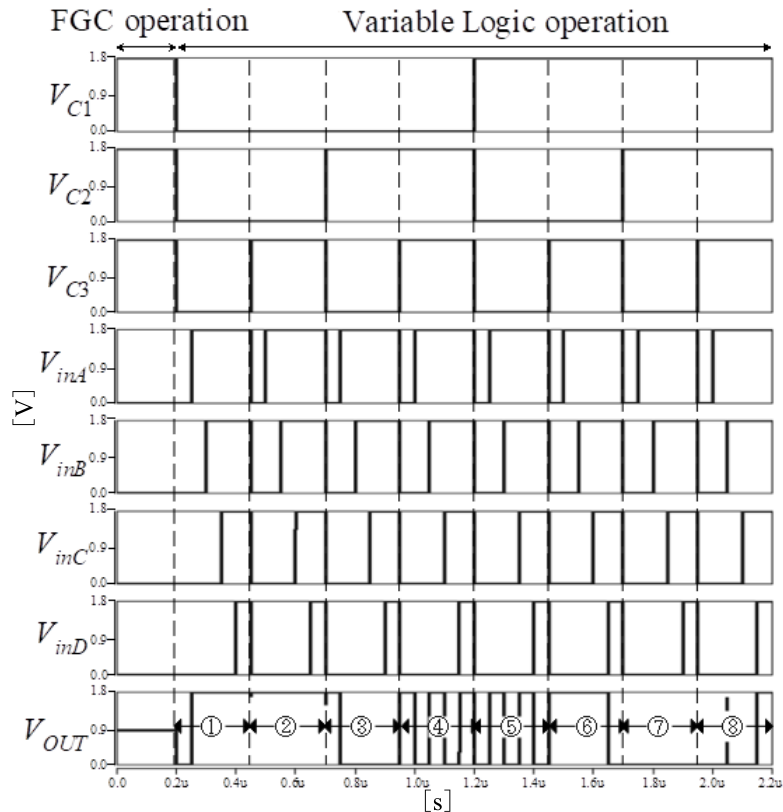| Symbol	Description	Value	Units
V_{DD}	Power supply voltage	1.8	V
GND	Ground voltage	0	V
W_n/L_n	Width/Length of nMOS	1.0/0.18	μm
W_p/L_p	Width/Length of pMOS	3.0/0.18	μm
$C_{Pi}, (i = 11 \sim 17, 21 \sim 26)$	Capacitance	16	fF
$C_{Mi}, (i = 1, 2, 3, 4, 5, 6, 7, 8)$	Capacitance	16	fF

FIGURE 5. Result of HSPICE simulation of the VLC

5. **Conclusions.** We explained the design method of νCMOS$_M$ of the 4-input variable logic circuit with FG calibration. Then, it was found that the VLC expresses eight logical functions, i.e., AND, OR, NAND, NOR, XOR, XNOR, Identity "1" and Identity "0".

In the future, we clarify the design method of νCMOS$_{P1}$ and νCMOS$_{P2}$ of the 4-input variable logic circuit with FG calibration. And this circuit will be converted into a chip and tested on an actual machine. And we will compare the performance with the 4-input LUT.

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