A STUDY OF A MINIMUM EUCLIDEAN DISTANCE SEARCH CIRCUIT FOR AN ASSOCIATIVE MEMORY

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Abstract. *Humans are good at association and recognition, and can instantly recall from the vast amount of information in their memory the most similar to the input information. This is due to the parallel operation of the human brain. However, if this function is attempted to be implemented in software, the search time increases rapidly as the number of bits and the amount of data to be compared increase. Therefore, associative memory, which is one of the functional memories that can retrieve not only the data that matches the input data but also the most similar data from a vast amount of data, has been attracting attention. We focused on neuron CMOS inverters, which have characteristics similar to a neuron in the brain, and hypothesized that a high-speed associative memory could be constructed by utilizing this element. In this study, we propose a minimum Euclidean distance search circuit in a minimum Euclidean distance search associative memory by utilizing neuron CMOS inverters. The proposed circuit can search for the most similar data using Euclidean distance as an indicator at high-speed. Furthermore, simulations of the proposed circuit are performed using HSPICE to confirm that the expected operations can be obtained by the proposed circuit.*
Keywords: Associative memory, Neuron CMOS inverter, Integrated circuit, Euclidean distance

1. **Introduction.** With the recent development of authentication systems and pattern matching technology, these technologies are expected to be applied to images and voice authentication, which are larger scale. In order to realize this system on a large scale, the function to rapidly search for the most similar data to the input data from the vast amount of data stored in the database is necessary, and the demand for this function is becoming higher and higher. Humans are also good at association and recognition, and when they see a partially hidden object, they can instantly recognize what it is from their vast memory. This is due to the parallel operation of the human brain. However, when

searching for data similar to the input data in software, the search time increases rapidly as the amount of data to be compared increases.

A solution to this problem is the use of associative memory [1-5]. This memory, in addition to the conventional memory function, is one of the functional memories that search at a high-speed for the most similar data as well as the exact match to the input data from a huge amount of data. We focused on a neuron CMOS (Complementary Metal-Oxide-Semiconductor) inverter which has characteristics similar to a neuron in the brain, and hypothesized that a high-speed associative memory could be constructed by utilizing this element [6].

We proposed a Euclidean distance detection circuit using the neuron CMOS inverters [7]. This circuit can detect the Euclidean distance between the input data and the reference data by converting the Euclidean distance to the time. A square calculation is required to obtain the Euclidean distance, but the circuit scale becomes large when this is realized with a digital circuit. Therefore, a minimum Euclidean distance search associative memory utilizing the current characteristics of MOS transistors with analog circuit has been proposed [8]. However, the conventional circuit may cause malfunctions due to variations of the MOS transistors in manufacturing and other factors. The proposed circuit uses the characteristics of the neuron CMOS inverter to perform this calculation, which makes circuit configuration simple and prevents malfunctions.

In this study, we propose a minimum Euclidean distance search circuit, which is an important functional circuit for retrieving the most similar data using Euclidean distance as an index in minimum Euclidean distance search associative memory, by using a Euclidean distance detection circuit with neuron CMOS inverters. The proposed minimum Euclidean distance search circuit is composed of the Euclidean detection circuits for the number of the reference data, and can compare all data in fully-parallel and search for the most similar data to the input data at high-speed.

For the more, in this study, simulations of the proposed circuit are performed using HSPICE to confirm that the proposed operations can be obtained by the proposed circuit.

2. Circuit Configuration.

2.1. **Euclidean distance detection circuit.** This section describes the Euclidean distance detection circuit that constitutes the minimum Euclidean distance search circuit using neuron CMOS inverters. The Euclidean distance detection circuit is a circuit that calculates the Euclidean distance of the reference data to the input data. Figure 1 shows a Euclidean distance detection circuit using a neuron CMOS inverter. The neuron CMOS
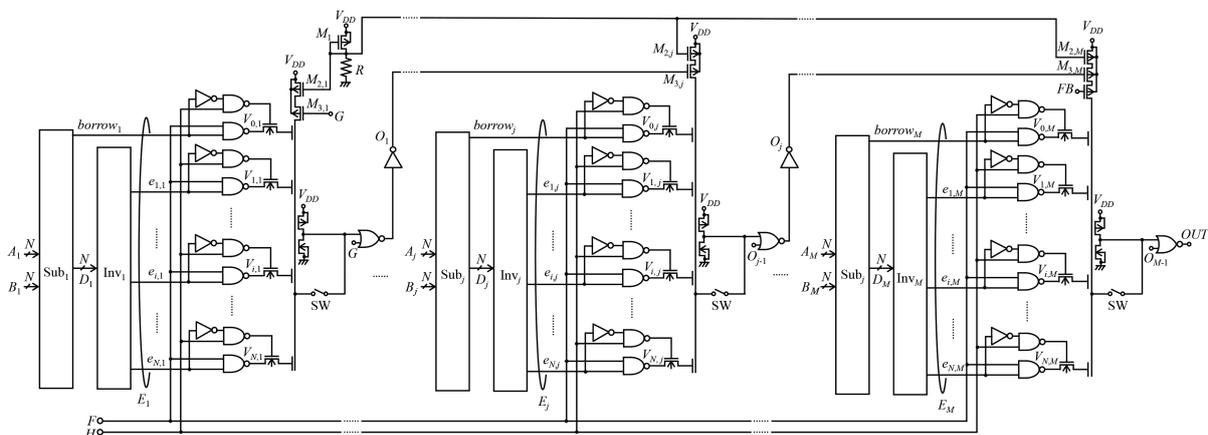

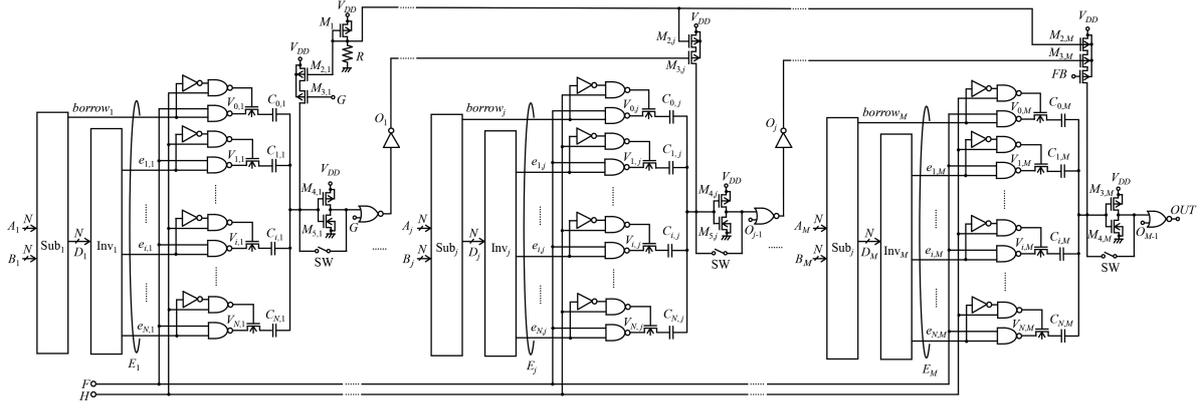FIGURE 1. Circuit configuration of a Euclidean distance detection circuit

FIGURE 2. Circuit configuration of the equivalent circuit of Figure 1

inverter is constructed by floating the input terminal of a conventional inverter and capacitively coupling multiple input terminals to it. Therefore, an equivalent circuit of the proposed circuit is shown in Figure 2. Note that the number of bits in the input and reference data is N and the number of elements is M. Here $\boldsymbol{A} = (A_1, \ldots, A_j, \ldots, A_M)$ is the input data and $\boldsymbol{B} = (B_1, \ldots, B_j, \ldots, B_M)$ is the reference data, and A_j and B_j are N-bit and M-element binary numbers, respectively. In order to obtain the Euclidean distance, first we find the difference of each element from the input data A_j and the reference data B_j. Next, the sum is calculated from the squared value of the difference. The Euclidean distance D_{Euc} is the square root from the value, and is defined by the following equation.

$$D_{Euc} = \sqrt{\sum_{i=1}^{M} |A_j - B_j|^2} \tag{1}$$

Since associative memory retrieves the data with the smallest Euclidean distance, there is no need to find the square root at the end in comparing their distances. Therefore, in this study, the square of the Euclidean distance is used as a measure of similarity retrieval.

$$D_{Euc}^2 = \sum_{i=1}^{M} |A_j - B_j|^2 \tag{2}$$

In these figures, V_{DD} is the supply voltage, and F, G, H, and FB are the control voltages. Sub_j is a circuit that outputs the result of subtraction of A_j and B_j. Inv_j is a circuit that outputs the value of Sub_j if the subtraction result is positive, and inverts D_j and outputs it if it is negative. When calculating $|A_j - B_{j,k}|$, if the subtraction result is negative, it is necessary to invert the result and add 1, but the most significant bit of the subtraction result is connected directly to the neuron CMOS inverter to solve the problem. These two circuits are used to calculate $|A_j - B_{j,k}|$.

Each switch is also composed of MOS transistors. SW is a switch to set the voltage V_F of the floating gate of the neuron CMOS inverter νCMOS to the threshold voltage V_{TH} of νCMOS. The capacitance $C_{0,j}$, $C_{i,j}$ between the floating gate of the νCMOS and input terminal shall be designed to satisfy the following equation.

$$C_{i,j} = 2^{i-1}C \tag{3}$$
$$C_{0,j} = C \tag{4}$$

Here, C is a unit capacitance.

The operation of this Euclidean distance detection circuit is described below. First, set the control voltage F to a low-level, G to a high-level, H to a low-level, and switch SW to ON. As a result, the voltage V_{Fj} of the floating gate of the νCMOS becomes the following equation.

$$V_{Fj} = V_{TH} \tag{5}$$

Next, we consider the change in the voltage V_{Fj} of the floating gate of νCMOS. The ΔV_{Fj}, amount of change in the floating gate voltage V_{Fj} when the voltage at the input terminal with input terminal-to-floating gate capacitance C_x changes by ΔV, is represented by the following equation.

$$\Delta V_{Fj} = \frac{C_x}{C_{Tj}} \Delta V \tag{6}$$

However, C_{Tj} in Equation (6) is the sum of the capacitances between the input terminal – the floating gate of νCMOS and is expressed as follows.

$$C_{Tj} = C_{0,j} + \sum_{i=1}^{N} C_{i,j} \tag{7}$$

Next, we consider the case where input data A_j and reference data B_j of element j are in disagreement and the jth bit $e_{i,j}$ of the difference E_j and the $borrow_j$ are a high-level. When the control voltage F is set to a high-level, the NAND outputs $V_{i,j}$ and $V_{0,j}$ change from the supply voltage V_{DD} to 0 V. If the floating gate voltage V_F at this time is V_F', then from Equations (5) and (6), V_F' can be expressed by the following equation.

$$V_{Fj}' = V_{Fj} - \frac{C_{0,j}}{C_{Tj}}(V_{DD} - V_{0,j}) - \sum_{i=1}^{N} \frac{C_{i,j}}{C_{Tj}}(V_{DD} - V_{i,j})$$

$$= V_{TH} - \frac{C_{0,j}}{C_{Tj}}(V_{DD} - V_{0,j}) - \sum_{i=1}^{N} \frac{C_{i,j}}{C_{Tj}}(V_{DD} - V_{i,j}) \tag{8}$$

Substituting Equations (3) and (4) into this equation yields the following equation.

$$V_{Fj}' = V_{TH} - \left\{ \frac{C}{C_{Tj}}(V_{DD} - V_{0,j}) - \sum_{i=1}^{N} \frac{2^{i-1}}{C_{Tj}}(V_{DD} - V_{i,j}) \right\}$$

$$= V_{TH} - \frac{C}{C_{Tj}}|A_j - B_{j,k}|V_{DD} \tag{9}$$

Next, the control voltage H is set to a high-level. $e_{i,j}$ is to a low-level, the capacitors $C_{i,j}$ are disconnected from the floating gate by the n-MOS transistors, and the total capacitance C_{Tj}' connected to the floating gate is expressed by the following equation.

$$C_{Tj}' = |A_j - B_{j,k}|C \tag{10}$$

Next, when the control voltage G is set to a low-level, MOS transistor $M_{3,1}$ turns ON and a constant current begins to flow from the current mirror circuit consisting of M_1, M_2 and R. As a result, the floating gate voltage V_{Fj} of the first stage begins to rise linearly from V_{Fj}'. The slope of the voltage rise at this moment becomes smaller in proportion to the difference. When this voltage exceeds the νCMOS threshold voltage V_{TH}, MOS transistors M_3 and M_2 turn ON and the second stage floating gate voltage V_{F2} rises linearly. Also, the slope of the voltage rise becomes smaller in proportion to the difference. By repeating this process, the Euclidean distance is converted into the time from when the control voltage G goes a low-level to when the output OUT goes a high-level. We describe the time it takes for the floating gate voltage V_{Fj}' to exceed the threshold voltage when a constant current I flows. The time T_j that takes for the floating gate voltage to exceed the threshold voltage is expressed by the following equation.

$$T_j = \frac{C_{Tj}' \left(V_{TH} - V_{Fj}' \right)}{I} \tag{11}$$

Substituting Equations (9) and (10) into this equation yields the following equation.

$$T_j = \frac{V_{TH} - \left\{V_{TH} - \frac{C^2}{C_{Tj}}|A_j - B_{j,k}|^2 V_{DD}\right\}}{I}$$

$$= \frac{V_{DD}}{I}\frac{C^2}{C_{Tj}}|A_j - B_{j,k}|^2 \tag{12}$$

The time T from when the control voltage G goes a low-level to when the output OUT goes a high-level can be expressed by the following equation.

$$T = \sum_{j=1}^{M} T_j = \sum_{j=1}^{M}\left\{\frac{V_{DD}}{I}\frac{C^2}{C_{Tj}}|A_j - B_{j,k}|^2\right\}$$

$$= \frac{V_{DD}}{I}\frac{C^2}{C_{Tj}}\sum_{j=1}^{M}|A_j - B_{j,k}|^2$$

$$= D_{Euc}^2 \frac{V_{DD}}{I}\frac{C^2}{C_T} \tag{13}$$

This equation shows that the time T from when the control voltage G goes a low-level to when the output OUT goes a high-level is not affected by parasitic capacitance and initial electrification. Also, from Equation (13), the time difference ΔT for a Euclidean distance different by 1 can be expressed by the following equation.

$$\Delta T = \frac{V_{DD}}{I}\frac{C^2}{C_T} \tag{14}$$

From the above, it can be seen that variations in the threshold voltage V_{TH} during temperature and manufacturing do not affect the difference in time relative to the Euclidean distance.

2.2. **Minimum Euclidean distance search circuit.** In this section, the proposed minimum Euclidean distance search circuit using neuron CMOS inverters is described. The minimum Euclidean distance search circuit finds the reference data that has the smallest Euclidean distance to the input data. Figure 3 shows a minimum Euclidean distance search circuit. Note that the number of bits of input and reference data is N, the number of elements is M, and the number of the reference data to be compared is L-words. Here $\boldsymbol{A} = (A_1, \ldots, A_j, \ldots, A_M)$ is the input data and $\boldsymbol{B}_k = (B_1, \ldots, B_j, \ldots, B_M)$ is the reference data, which are N-bit and M-element binary numbers, respectively. Also, $\boldsymbol{B}_k$ ($k = 1, 2, \ldots, L$) is the L-word reference data to be compared with the input data $\boldsymbol{A}$. FB is the control voltage that stops the operation of all Euclidean distance detection circuits. The proposed circuit consists of L-word Euclidean distance detection circuits described in Section 2.1.

The Euclidean distance detection circuit used in the minimum Euclidean distance search circuit converts the Euclidean distance to time. The output OUT_k of the Euclidean distance detection circuit at the reference data point with the smallest Euclidean distance goes a high-level first. When any one output OUT_k goes a high-level, a high-level is output from the multi-input OR circuit. The output of the multi-input OR circuit is input to the FB of all Euclidean distance detection circuits, which stops the operation of all Euclidean distance detection circuits. From this, OUT_k at the reference data point with the smallest Euclidean distance to the input data goes a high-level. With the above operation, the proposed minimum Euclidean distance search circuit can detect the reference data with the smallest Euclidean distance to the input data.
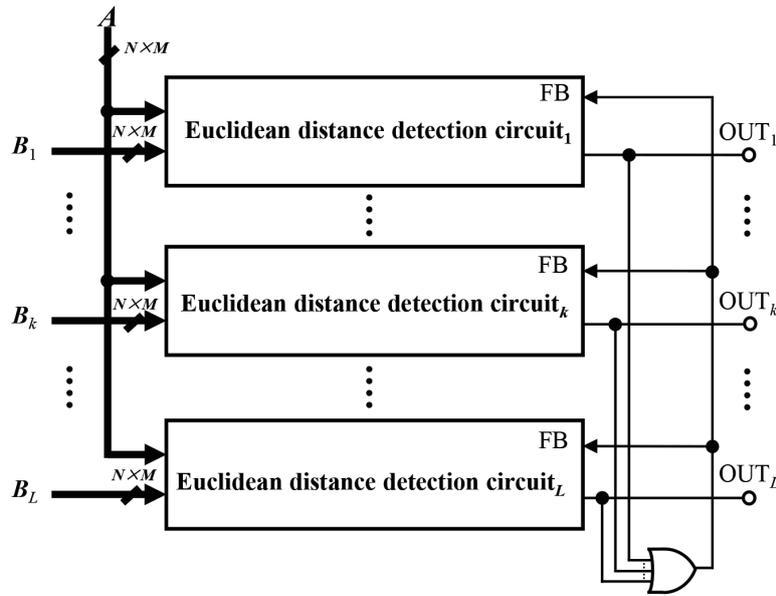
FIGURE 3. Circuit configuration of a minimum Euclidean distance search circuit

3. **Simulation Results.** Simulation results for the minimum Euclidean distance search circuit proposed in Section 2.2 are presented. The circuit was designed using Cadence's IC Virtuoso Schematic Editor and simulated using Synopsys' HSPICE. The Rohm Semiconductor 0.18 μm CMOS process was used as the SPICE parameters. The supply voltage V_{DD} was set to 1.8 V and the threshold voltage V_{TH} for the floating gate of the neuron CMOS inverter was designed to be 0.9 V as half of the supply voltage.

Figure 4 shows the simulation results of the floating gate voltage V_F of the Euclidean distance detection circuit set so that the Euclidean distances from the input data are $\sqrt{1}$, $\sqrt{2}$, $\sqrt{4}$ and $\sqrt{8}$, respectively. The equivalent circuit shown in Figure 2 was used for the simulation, and the reference data was set to 4-bits and 4-elements. It can be seen that the floating gate voltage V_F falls by the magnitude of the difference between A_j and B_j and then rises linearly due to the constant current flowing from the current mirror circuit. Also, the slope of the voltage rise becomes smaller in proportion to the difference.
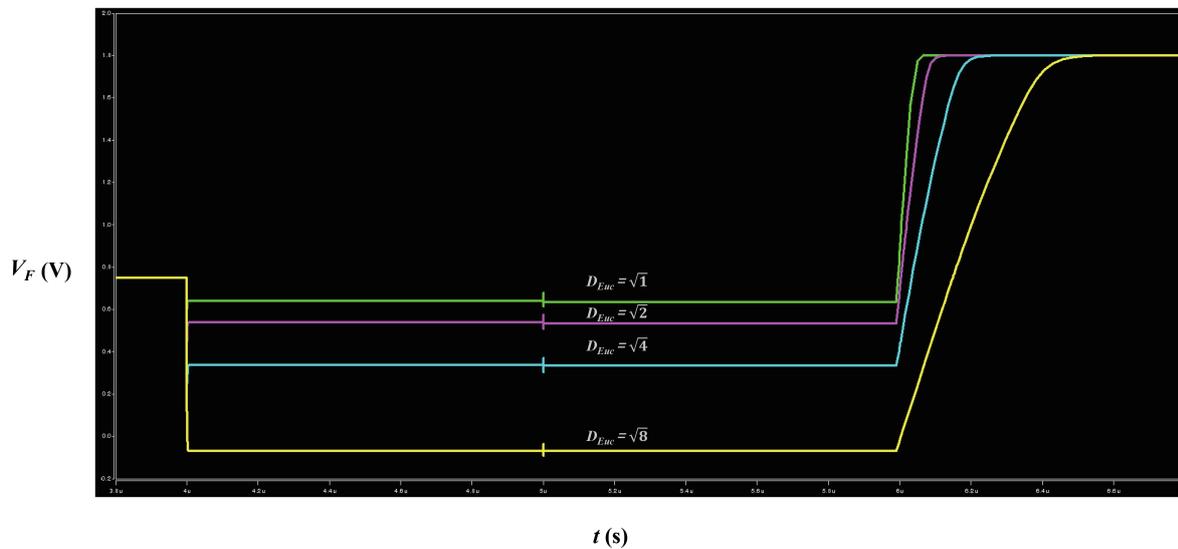

FIGURE 4. Simulation result of Euclidean distance detection circuit

Figure 5 shows the simulation results of OUT_k of the proposed circuit with 8-words, 3-elements, and 4-bits using the setting of Table 1. This figure shows that OUT_2 which has the smallest Euclidean distance becomes a high-level, indicating that the proposed circuit can achieve the expected operations.
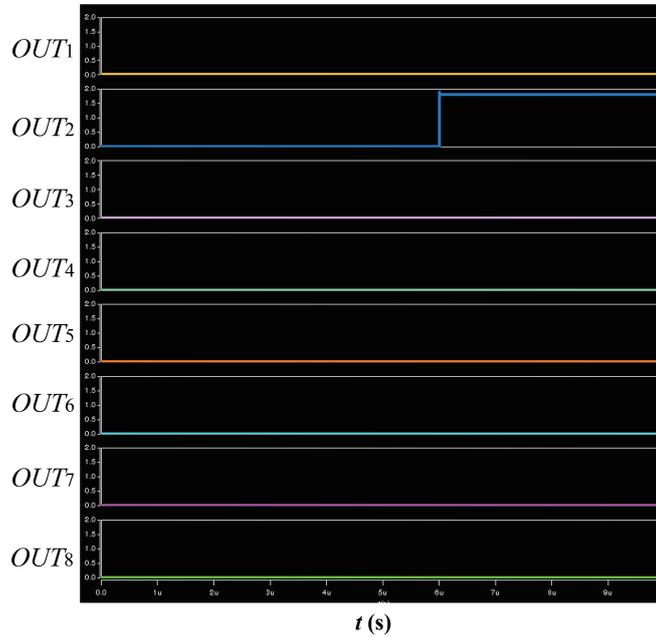

FIGURE 5. Simulation result of the proposed circuit

TABLE 1. An example of the I/O data in SPICE simulations

Input data	Reference data	Euclidean distance	Output
	$\boldsymbol{B}_1$ ($B_{1,1} = 1$, $B_{2,1} = 1$, $B_{3,1} = 1$)	$\sqrt{5}$	OUT_1
	$\boldsymbol{B}_2$ ($B_{1,2} = 1$, $B_{2,2} = 2$, $B_{3,2} = 1$)	$\sqrt{4}$	OUT_2
	$\boldsymbol{B}_3$ ($B_{1,3} = 1$, $B_{2,3} = 2$, $B_{3,3} = 0$)	$\sqrt{9}$	OUT_3
$\boldsymbol{A}$ ($A_1 = 1$, $A_2 = 2$, $A_3 = 3$)	$\boldsymbol{B}_4$ ($B_{1,4} = 1$, $B_{2,4} = 3$, $B_{3,4} = 0$)	$\sqrt{10}$	OUT_4
	$\boldsymbol{B}_5$ ($B_{1,5} = 1$, $B_{2,5} = 4$, $B_{3,5} = 0$)	$\sqrt{13}$	OUT_5
	$\boldsymbol{B}_6$ ($B_{1,6} = 2$, $B_{2,6} = 4$, $B_{3,6} = 0$)	$\sqrt{14}$	OUT_6
	$\boldsymbol{B}_7$ ($B_{1,7} = 3$, $B_{2,7} = 4$, $B_{3,7} = 0$)	$\sqrt{17}$	OUT_7
	$\boldsymbol{B}_8$ ($B_{1,8} = 4$, $B_{2,8} = 4$, $B_{3,8} = 0$)	$\sqrt{22}$	OUT_8

From the above results, the Euclidean distance detection circuit converts the Euclidean distance between input data and reference data into a time difference, and the proposed minimum Euclidean distance search circuit can detect the most similar data by using this time.

4. **Conclusion.** In this study, we proposed a minimum Euclidean distance detection circuit based on a neuron CMOS inverter. The proposed circuit converts the Euclidean distance into the time required for all Euclidean distance detection circuits to stop, and by comparing the time, it can detect the reference data with the smallest Euclidean distance to the input data.

Furthermore, simulations using HSPICE have confirmed that the proposed circuit can achieve the proposed operations.

In the future, we would like to design registers, address decoders and so on and configure a minimum Euclidean distance search associative memory with the proposed circuit. In addition, we are set to integrate the associative memory and experiment using the prototype chip.

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